Issue 1c

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Assembly and Test Houses:

N-CHANNEL RADIATION TOLERANT POWER MOSFET BASED ON TYPE L1056

Detail Specification

Issue 1c

Deutsches Zentrum
für Luft- und Raumfahrt e.V.

German
Aerospace Center.

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1 General

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data for radiation tolerant N-Channel Power MOSFET, based on Lewicki Type L1056 (based on HUF75639). The total dose hardness of 30 kRad can be expected. It shall be read in conjunction with DLR Generic Specification DLR-RF-PS-STD-006, the requirements of which are supplemented herein.

1.2 Component Type Variants

Variants of the basic type transistors specified herein, which are also covered by this specification, are listed in table 1(a).

1.3 Maximum Ratings

The maximum ratings for the Power MOSFET specified herein, which shall not be exceeded at any time during use or storage, are as scheduled in table 1(b).

1.4 Parameter Derating Information

The parameter derating information for the Power MOSFET specified herein is shown in figure 1(a). The Safe Operating Area information is shown in figure 1(b).

1.5 Physical Dimensions

The physical dimensions for the Power MOSFET specified herein are shown in figure 2(a), figure 2(b) and figure 2(c).

1.6 Functional Diagram

The functional diagram for the Power MOSFET specified herein, including lead identification, is shown in figure 3.

1.7 Handling Precautions

1.7.1 ESD Precaution

The Power MOSFET specified herein is susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling. Power MOSFET is categorized in Class 1, with a minimum critical path failure voltage of 1000 V.

1.7.2 Electrical Precaution

Never insert the MOSFET into the circuit when voltage is applied. When applying bias to the MOSFET first apply gate voltage then drain voltage. Avoid turning the instrument power on and off or switching between instrument ranges when bias is applied to the MOSFET. Transient generated in the vicinity must be eliminated.

Table 1(a) – Type Variants

	(01)	(02)	(03)	(04)	(05)	(06)	(07)	(08)	(09)	(10)
Variant / Type Note 1	Package Type	Based on Type	ID (MAX.) [A] Note 2	ID (MAX.) [A] Note 3	IS [A] Note 2	VDS [V]	IDM(MAX) [Apk] Note 4	VDG [V]	Ptot [W] Note 2	RTH (J-C) [K/W]
01	TO257	HUF75639	20	12.5	20	100	80	+/- 20	75	1.7
02	SMD05	HUF75639	30	18.7	30	100	88	+/- 20	75	1.7
03	SMD2	HUF75639	56	35	56	100	100	+/- 20	200	0.6

NOTES:

1. Variant 01 = L1056-257; Variant 02 = L1056-005; Variant 03 = L1056-020
2. Tcase = 25 °C (thermally conductive mounted to a liquid cooled heat sink)
3. Tcase = 100 °C (thermally conductive mounted to a liquid cooled heat sink)
4. Repetitive rating; pulse width limited by maximum junction temperature

Table 1(b) – Maximum Ratings

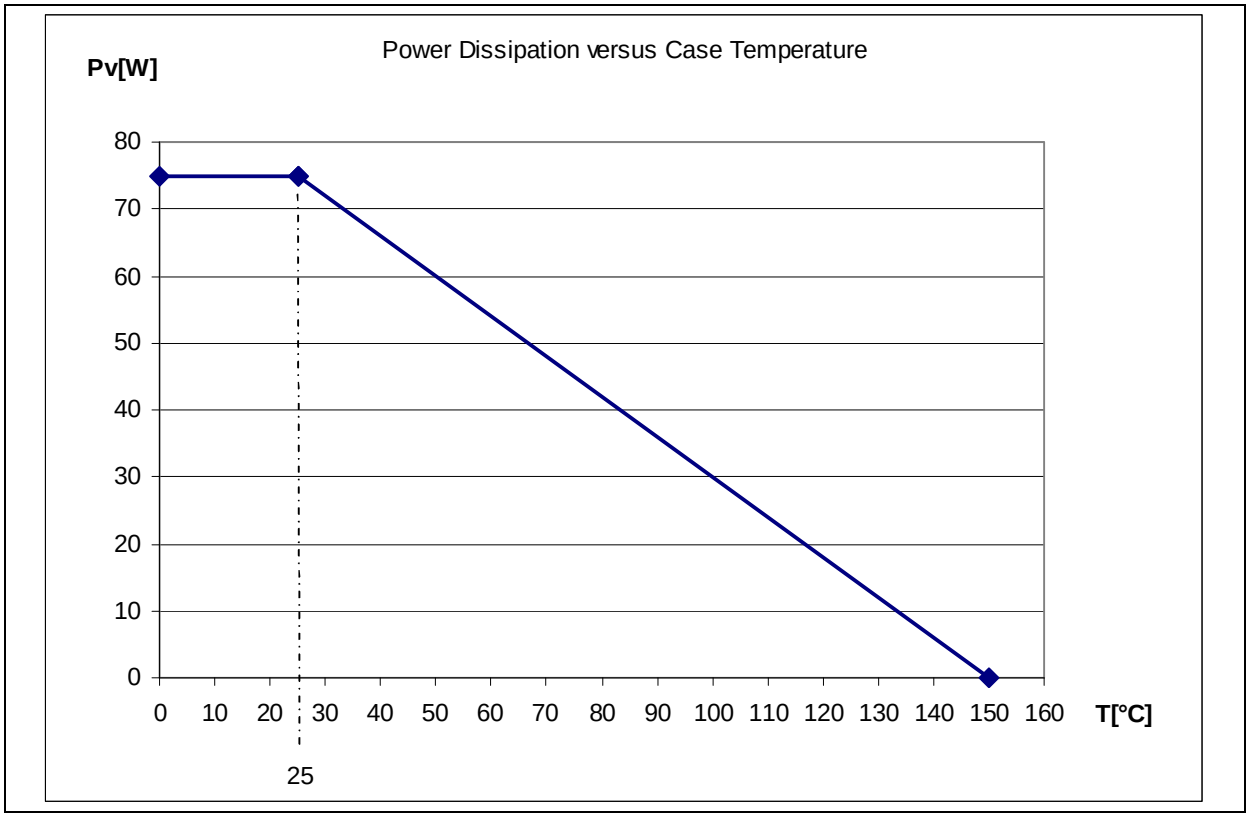
No.	Characteristics	Symbol	Maximum Ratings	Unit	Remarks
1	Drain Source Voltage	VDS	100	V	
2	Gate Source Voltage	VGS	+/- 20	V	
3	Drain Gate Voltage	VDG	Table 1(a) Column (08)	V	
4	Drain Current (Continuous)	ID	Table 1(a) Column (03)	A	at Tcase=+25 °C
5	Drain Current (Continuous)	ID	Table 1(a) Column (04)	A	at Tcase=+100 °C
6	Source Current (Continuous)	IS	Table 1(a) Column (05)	A	at Tcase =+25 °C
7	Drain Current Pulsed (Peak)	IDM	Table 1(a) Column (07)	Apk	
8	Total Power Dissipation	Ptot	Table 1(a) Column (09)	W	Note 1
9	Operating Temperature Range	Top	-55 to +150	°C	Tamb
10	Storage Temperature Range	Tsto	-55 to +150	°C	
11	Soldering Temperature	Tsol	+260	°C	Note 2
12	Thermal Resistance (Junction to Case)	Rth(J-C)	Table 1(a) Column (10)	K/W	

NOTES:

1. For derating, see figure 1(a)
2. Variant 01: Duration 10 seconds maximum at distance of not less than 1.5 mm from the device body and the same termination shall not be resoldered until 3 minutes have elapsed.
   Variant 02 and Variant 03: Duration 10 seconds maximum. The same termination shall not be resoldered until 3 minutes have elapsed.

Figure 1(a) - Parameter Derating Information

Variant 01 and 02



Variant 03

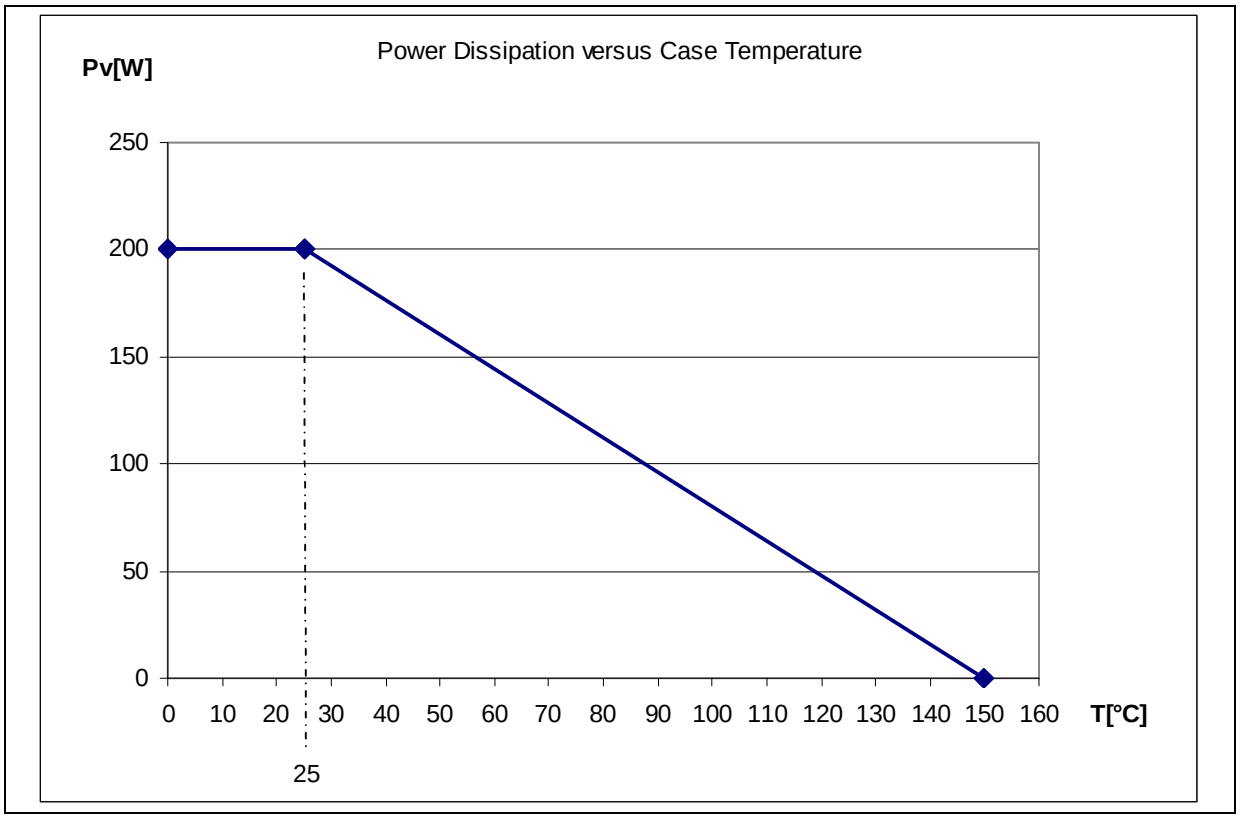
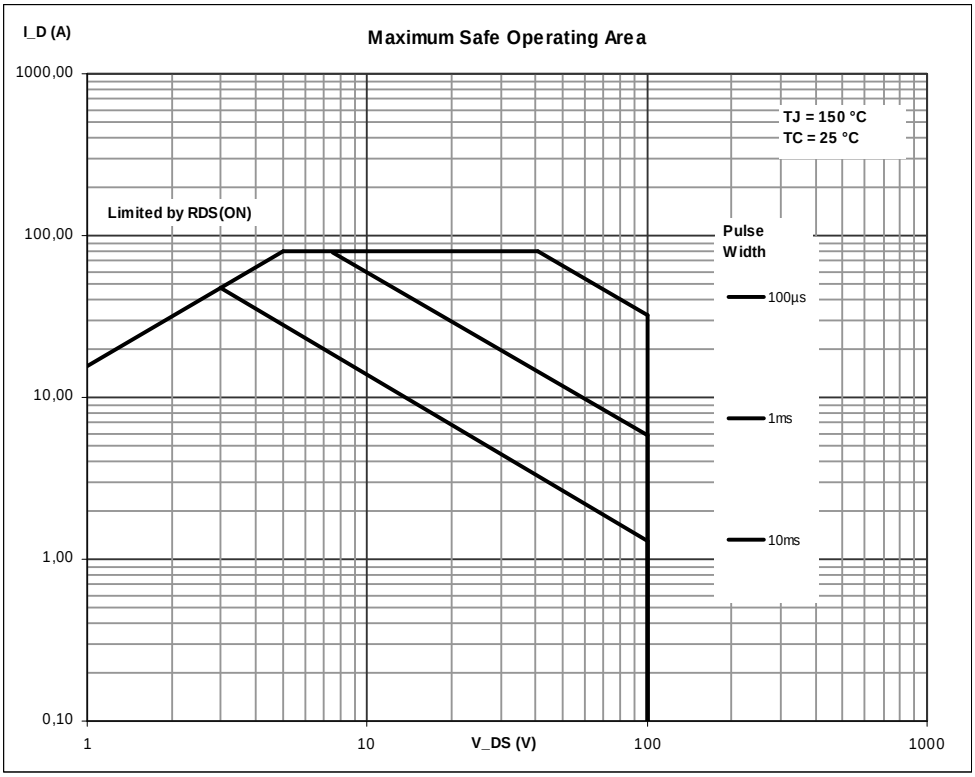
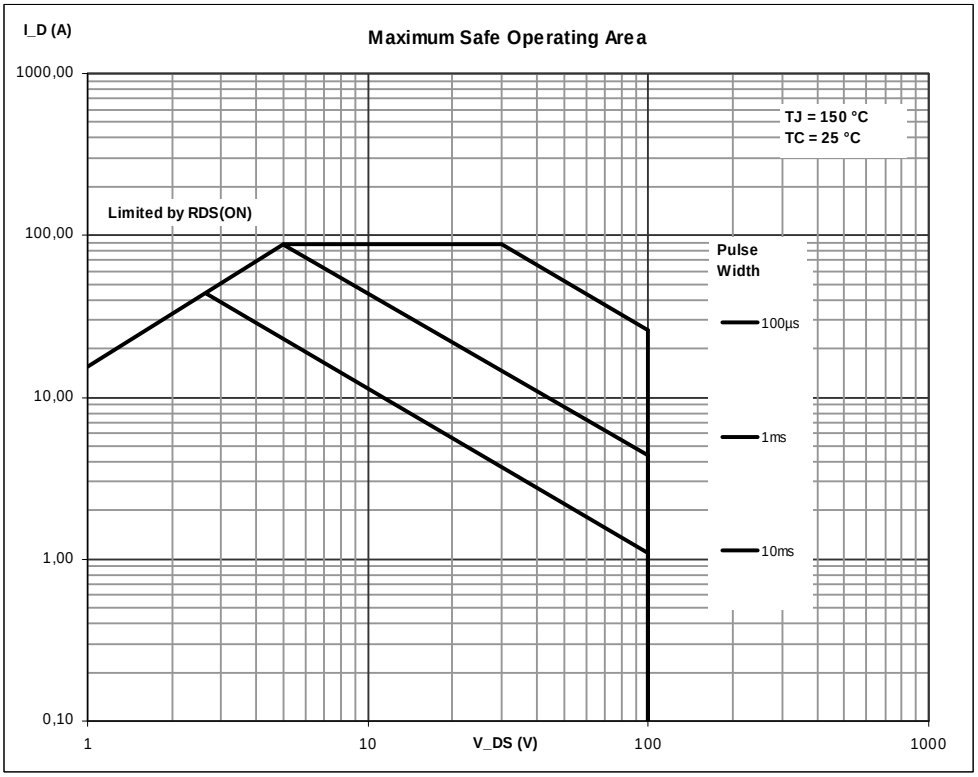


Figure 1(b) – Maximum Safe Operating Area

Variant 01



Variant 02



Variant 03

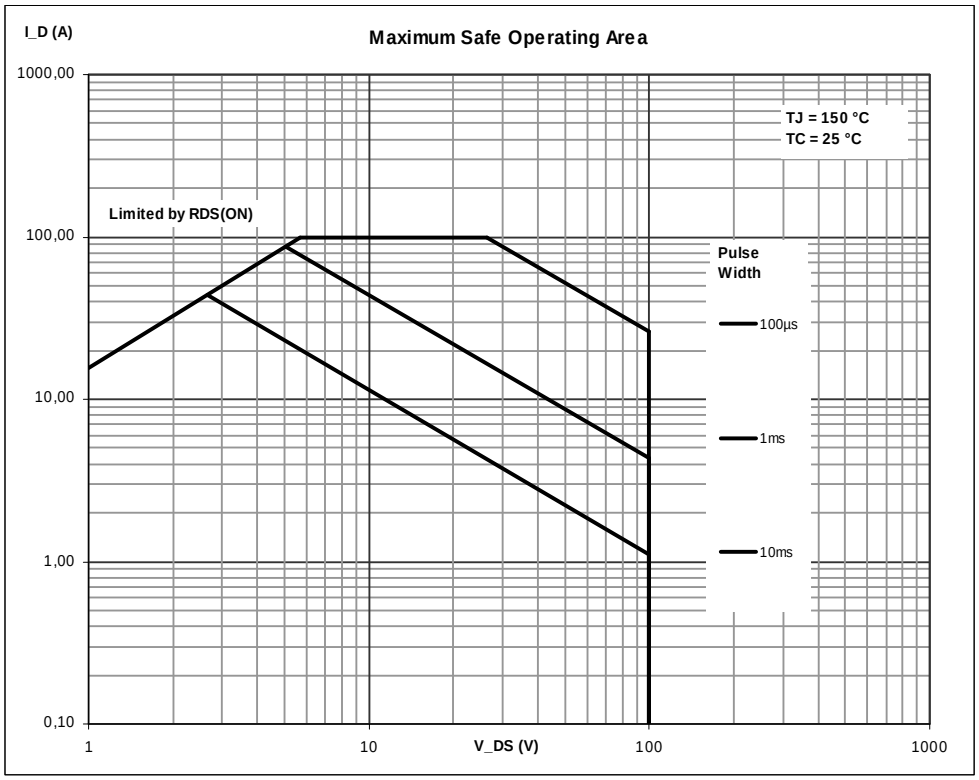
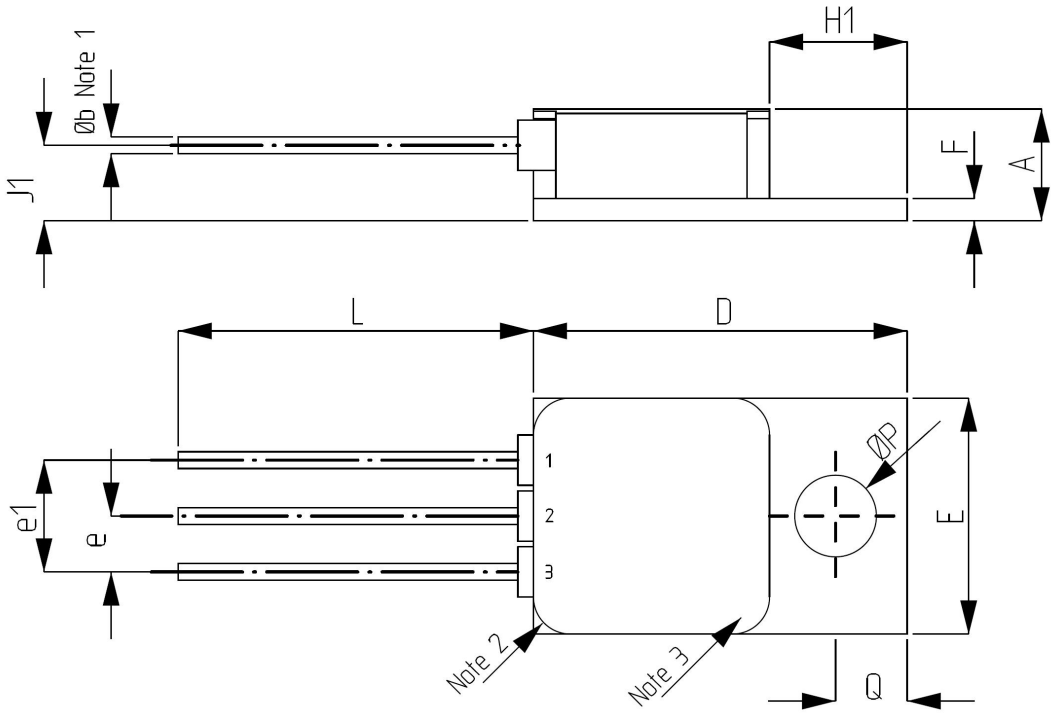

I_D (A)
Maximum Safe Operating Area
1000,00
100,00
10,00
1,00
0,10
1
10
V_DS (V)
100
1000
TJ = 150 °C
TC = 25 °C
Limited by RDS(ON)
Pulse
Width
100µs
1ms
10ms

Figure 2 - Physical Dimension
Variant 01



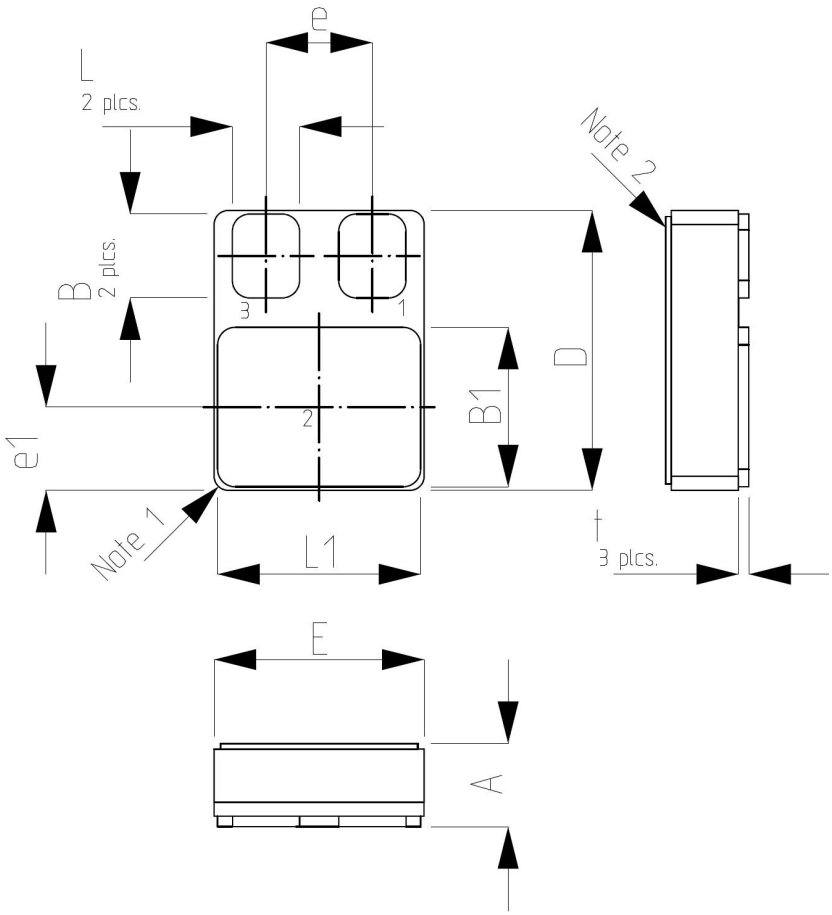
Package contains BeO substrate

Pos.	Symbol	Dimensions [mm]	
		Min.	Max.
1	A	4.8	5.3
2	Øb	0.63	0.89
3	D	16.41	16.91
4	E	10.29	10.79
5	e	2.4	2.74
6	e1	4.88	5.28
7	F	0.75	1.25
8	H1	5.75	6.25
9	J1	2.75	3.25
10	L	15.62	16.12
11	ØP	3.35	3.85
12	Q	2.87	3.37

NOTES:

1. All 3 leads
2. Corner radii from R1.4 to R1.9
3. Marking according to paragraph 4.5

Variant 02

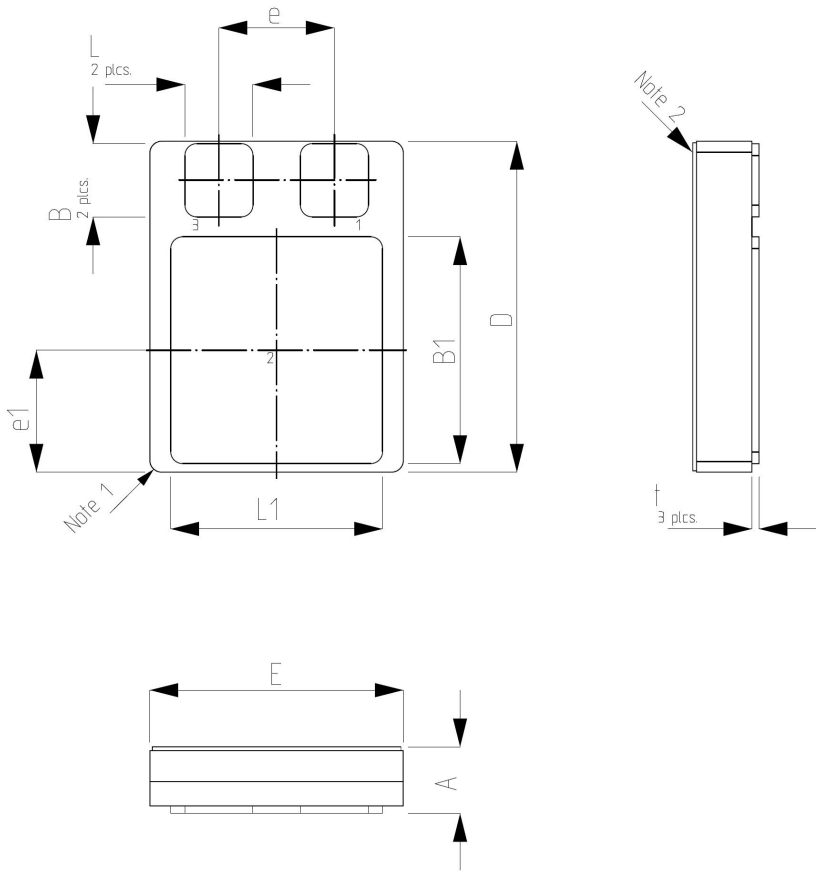


Pos.	Symbol	Dimensions [mm]	
		Min.	Max.
1	A	2.34	2.94
2	B	2.8	3.3
3	B1	5.47	5.97
4	D	10.03	10.29
5	E	7.4	7.6
6	e	3.68	3.94
7	e1	2.6	2.86
8	L	2.29	2.54
9	L1	7.1	7.6
10	t	0.25	0.5

NOTES:

1. Corner radii from R0.3 to R0.7
2. Marking according to paragraph 4.5

Variant 03

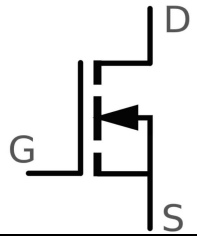


Pos.	Symbol	Dimensions [mm]	
		Min.	Max.
1	A	3.31	3.91
2	B	3.69	4.29
3	B1	11.77	12.37
4	D	17.31	17.91
5	E	13.1	13.7
6	e	5.8	6.4
7	e1	6.15	6.75
8	L	3.26	3.66
9	L1	10.88	11.48
10	t	0.25	0.5

NOTES:

1. Corner radii max R0.635
2. Marking according to paragraph 4.5

Figure 3 – Functional Diagram



Terminal	**Variant 01** L1056-257	**Terminal**	**Variant 02** L1056-005	**Terminal**	**Variant 03** L1056-020
1	Gate	1	Gate	1	Gate
2	Drain	2	Drain	2	Drain
3	Source	3	Source	3	Source

NOTES:

1. Variant 01 (L1056-257): Due to the insert BeO package the drain is electrically isolated from the case
2. Variant 02 (L1056-005) and Variant 03 (L1056-020): Due to the insert Al2O3 packages the drains are electrically isolated from the cases

2 Applicable Documents

The following specifications and standards form a part of this specification to the extend specified herein.

1	DLR-RF-PS-STD-006	Discrete Semiconductor Components
2	ESCC 21300	Terms, Definition, Abbreviations Symbols and Units
3	ESCC 21700	General Requirements for the Marking of ESCC Components
4	ESCC 22900	Total Dose Steady – State Irradiation
5	ESCC 23500	Requirements for Lead Materials and Finishes for Components for Space Application
6	MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
7	MIL-STD-750	Test Methods and Procedures for Semiconductor Devices
8	MIL-STD-883	Test Methods Standards, Microcircuits

3 Terms, Definitions, Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definition, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

BVGSS	Gate to Source Breakdown Voltage
CISS	Common Source Input Capacitance
COSS	Common Source Output Capacitance
CrSS	Common Source Output Transfer Capacitance
DUT	Device under test
ESCC	European Space Components Coordination
gfs	Forward Transfer Conductance
HTGB	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
ID	Drain Current
IGSS	Gate to Source Leakage Current
IS	Source Current
MIL – STD, TM	Military Standard Test Method
OFHC	Oxygen Free High thermal Conductivity
SOA	Safe Operating Area
VDG	Drain to Gate Voltage
VDS	Drain to Source Voltage
VGS	Gate to Source Voltage
VGS(th)	Gate Threshold Voltage
VSD	Source to Drain Diode Forward Voltage
Ri	Insulated Resistance, Pins to case

4 Requirements

4.1 General

The complete requirements for procurement of the Power MOSFET specified herein are stated in this specification and Generic Specification DLR-RF-PS-STD-006 for discrete semiconductor components. Deviations from the Generic Specification DLR-RF-PS-STD-006 applicable to this specification are listed in the following paragraph 4.2.

4.2 Deviations / Amendments from Generic Specification DLR-RF-PS-STD-006

4.2.1 Deviations from Production Controls (Chart F2)

- Wafer Lot Acceptance Test is replaced by an Incoming Inspection at the Assembly & Testhouse. Incoming Inspection shall be in accordance with DLR-RF-PS-STD-006 paragraph 4.7.9. Hereby the visual inspection is performed on all samples (100 % inspection) and the die attach and bondability is tested on 3 samples.

4.2.2 Deviations from Screening Tests (Chart F3)

- The HTRB of paragraph 8.20 of DLR-RF-PS-STD-006 is performed for 168 h and not for 48 h.
- The Power Burn-In of paragraph 8.21 of DLR-RF-PS-STD-006 is replaced by HTGB as specified in table 5(b) herein.

4.2.3 Deviations from Capability Approval, Capability Approval Maintenance and Lot Validation test (Chart F4)

- The sample size from subgroup 2 will be increased from 15 to 20 samples.
- Subgroup 2 is divided into subgroup 2(a) Operation Life with 10 samples and subgroup 2(b) Intermittent Life with 10 samples. For subgroup 2(b) measurements performed after 0, 2000 and 6000 cycles. Conditions see table 5(c) and table 5(d).
- After completion of subgroup 2, 5 test samples from subgroup 2(b) are used for subgroup 3.
- Permanence of marking of paragraph 8.17 of DLR-RF-PS-STD-006 is not applicable.

4.3 Mechanical Requirements

4.3.1 Dimension Check

The dimensions of the Power MOSFET specified herein shall be checked on sample base. They shall conform to those shown in figure 2(a), figure 2(b) and figure 2(c).

4.3.2 Weight

The maximum weight of the Power MOSFET specified herein is:

Type	Package	Weight [g]
L1056-257	TO257	5
L1056-005	SMD05	1.2
L1056-020	SMD2	5.5

4.3.3 Terminal Strength

For Terminal Strength a solid copper wire is soldered to the pad respectively the specified weight shall be applied to each lead. The requirements for Variants 01 are specified in MIL-STD-750 TM 2036, test condition A and for Variant 02 and 03 the requirements of MIL-STD-883 TM 2004, test condition D (solder pad adhesion for leadless chip carrier and similar devices) are applicable. The applied force and duration are as follows:

Variant 01: Applied force 20 N, duration 15 s
Variant 02: Applied force 10 N, duration 30 s
Variant 03: Applied force 20 N, duration 30 s

4.3.4 Coating of internal cavity

Chip coating is not applicable.

4.4 Materials and Finishes

The material and finish shall be as specified herein. Where a definite material is not specified, a material which will enable the MOSFET specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Package	Type	Materials and finishes
TO257	L1056-257	Body: CuW Alloy Frame: OFHC Cu Au plate 1.27 µm min over min 1.27 µm Ni
		Lid: Kovar Au plate 1.27 µm min over min 2 µm Ni
SMD05	L1056-005	Body: ceramic Al2O3 Frame: Kovar Au plate 1.27 µm min over 2.54 µm Ni
		Lid: Kovar Au plate 0.2 µm min over min 1.27 µm Ni
SMD2	L1056-020	Body: ceramic Al2O3 Frame: Kovar Au plate 1.27 µm min over min 2.54 µm Ni
		Lid: Kovar Au plate 0.2 µm min over min 1.27 µm Ni

The packages are hermetically sealed: 1E-08 atm cc / s

4.4.2 Terminal Material and Finishes

Variant 01

The pin material is copper-core, iron nickel alloy 52, clad-ratio 3:1 and in accordance with the requirements of ESCC Basic Specification No. 23500 type ‘H’. Pins are plated with min 1.27 µm Au over min 1.27 µm Ni.

Variant 02 and Variant 03

The terminal material is CuW and in accordance with the requirements of ESCC Basic Specification No. 23500 type ‘Q’ and type ‘14’ finish. Terminals are plated with min 2.54µm Au over min 1.27µm Ni.

4.5 Marking

4.5.1 General

The components specified herein are marked in accordance with the requirements of ESCC Basic Specification No. 21700. The information to be marked and the order of precedence, is as follows:

- DLR Component Number and Logo (in case this part type is covered by capability approval)
- Traceability Information
- Identification of hazardous substances as for L1056-257

4.5.2 Lead Identification

Lead Identification shall be as in figure 2 and figure 3.

4.5.3 DLR Component Number

Each component shall bear the DLR component number which shall be constituted and marked as follows:

DLR-RF-PS-STD-016	-	0X
DLR component number		Variant Identification 01 = L1056-257; 02 = L1056-005; 03 = L1056-020

4.6 Electrical Measurements

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in table 2, table 6 and table 7.
Unless otherwise specified, the measurements have been performed at Tamb = 25 °C +/- 5 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured in respect of electrical characteristics are scheduled in table 3. The measurements have been performed at Tamb = 125 °C +0 °C/-5 °C and Tamb = -55 °C +5 °C/-0 °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements are listed in figure 4 of this specification.

4.7 Screening Tests

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in table 4 of this specification. Unless otherwise stated, measurements shall be performed at Tamb = 25 °C +/- 5 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift values requirements, the appropriate limit value specified for a given parameter in table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn In (HTRB)

The requirements for the HTRB burn-in are specified in MIL-STD-750 TM 1042 test condition A (steady – state gate bias) and as specified in table 5(a) of this specification.

4.7.3 Conditions for High Temperature Gate Bias Burn In (HTGB)

The requirements of the HTGB burn-in are specified in MIL-STD-750 TM 1042 test condition B (steady – state gate bias) and as specified in table 5(b) of this specification.

4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn In (HTRB)

The electrical circuit for HTRB is shown in figure 5(a) of this specification.

4.7.5 Electrical Circuit for High Temperature Gate Bias Burn In (HTGB)

The electrical circuit for HTGB is shown in figure 5(b) of this specification.

4.7.6 Verification of Safe Operating Area

As specified in paragraph 8.22 of Generic Specification the test is performed in accordance with MIL-STD-750 TM 3474 and as specified below. Figure 4(a) shows the electrical circuit for verification of SOA. At the case temperature Tc = 25 °C ten pulses for the maximum allowed current at VDS = 80 % of the maximum rated VDS and at 10 ms as given in figure 1(b) has to be applied. The time between each pulse shall such that the part can cool down at room temperature. After 10 pulses are applied table 2(a) except no. 9 shall be measured. All failed parts shall be removed from the lot.

Table 2(a) – Electrical Measurements at Room Temperature / DC Parameters

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
1	Breakdown Voltage Drain Source	BVDSS	3407 Bias Condition 'C'	ID=250 µA VGS=0 V	100	-	V
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS	2	4	V
3	Forward Gate to Source Leakage Current	IGSSF	3411	VGS=20 V	-	100	nA
4	Reverse Gate to Source Leakage Current	IGSSR	3411	VGS=-20 V	-100	-	nA
5	Drain Current	IDSS	3413 Bias Condition 'C'	VGS=0 V VDS=Note 2	-	250	µA
6	Drain Source On Resistance	RDS(ON)	3421	ID=20 A VGS=10 V Note 1 Variant 01	-	0.04	Ω
				Variants 02, 03	-	0.03	Ω
7	Drain Source On Voltage	VDS(ON)	3405	ID=20 A VGS=10 V Note 1	-	1	V
8	Source to Drain Diode Forward Voltage	VSD	4011	IS= 20 A VGS=0 V Note 1	0.5	1.5	V
9	Insulation Resistance	Ri	MIL-STD-202 TM302 Condition 'C'	Note 3	100	-	MΩ

NOTES:

1. Pulsed measurement: pulse width ≤ 100 µs, duty cycle ≤ 1 %
2. VDS (80 %) = 80 V
3. Between linked terminals and case, electrification time ≥ 1 s
4. Thermal impedance has to be measured only one time

Table 2(b) – Electrical Measurements at Room Temperature / AC Parameters

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
10	Forward Transconductance	gfs	3475	ID=10 A VDS=10 V Note 1	6	-	S
11	Turn-on Delay Time	td(ON)	3472 and figure 4(b) below	RG=5 Ω ID=10 A VGS=0 V / 10 V VDD=50 V	-	30	ns
12	Rise Time	tr	3472 and figure 4(b) below	RG=5 Ω ID=10 A VGS=0 V / 10 V VDD=50 V	-	60	ns
13	Turn-off Delay Time	td(OFF)	3472 and figure 4(b) below	RG=5 Ω ID=10 A VGS=0 V / 10 V VDD=50 V	-	70	ns
14	Fall Time	tf	3472 and figure 4(b) below	RG=5 Ω ID=10 A VGS=0 V / 10 V VDD=50 V	-	30	ns
15	Common Source Input Capacitance	Ciss	3431	VDS=25 V VGS=0 V f=1 MHz	-	2500	pF
16	Common Source Output Capacitance	Coss	3453	VDS=25 V VGS=0 V f=1 MHz	-	600	pF
17	Common Source Reverse Transfer Capacita	Crss	3433	VDS=25 V VGS=0 V f=1 MHz	-	150	pF
18	Thermal Impedance	Zth	3161	tH=10 ms tMD=30 µs tSW=10 µs IH=1 A VH=30 V Note 4 Variant 01	-	0.75	K/W
				Variants 02, 03	-	0.55	K/W
19	Thermal Impedance	Zth	3161	tH=30 ms tMD=30 µs tSW=10 µs IH= 1A VH=30 V Note 4 Variant 01	-	1.33	K/W
				Variants 02, 03	-	0.77	K/W

NOTES: see Notes of table 2(a)

Table 3(a) – Electrical Measurements at High Temperature (Ta = 125 °C +0 °C/-5 °C)

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS	1.5	4	V
3	Forward Gate to Source Leakage Current	IGSSF	3411	VGS=20 V	-	200	nA
4	Reverse Gate to Source Leakage Current	IGSSR	3411	VGS=-20 V	- 200		nA
5	Drain Current	IDSS	3413 Bias Condition 'C'	VGS=0 V VDS=Note 3	-	1000	µA
6	Drain Source On Resistar	rDS(ON)	3421	ID=20A VGS=10 V Note 1 Variant 01	-	0.07	Ω
				Variants 02,03	-	0.05	Ω

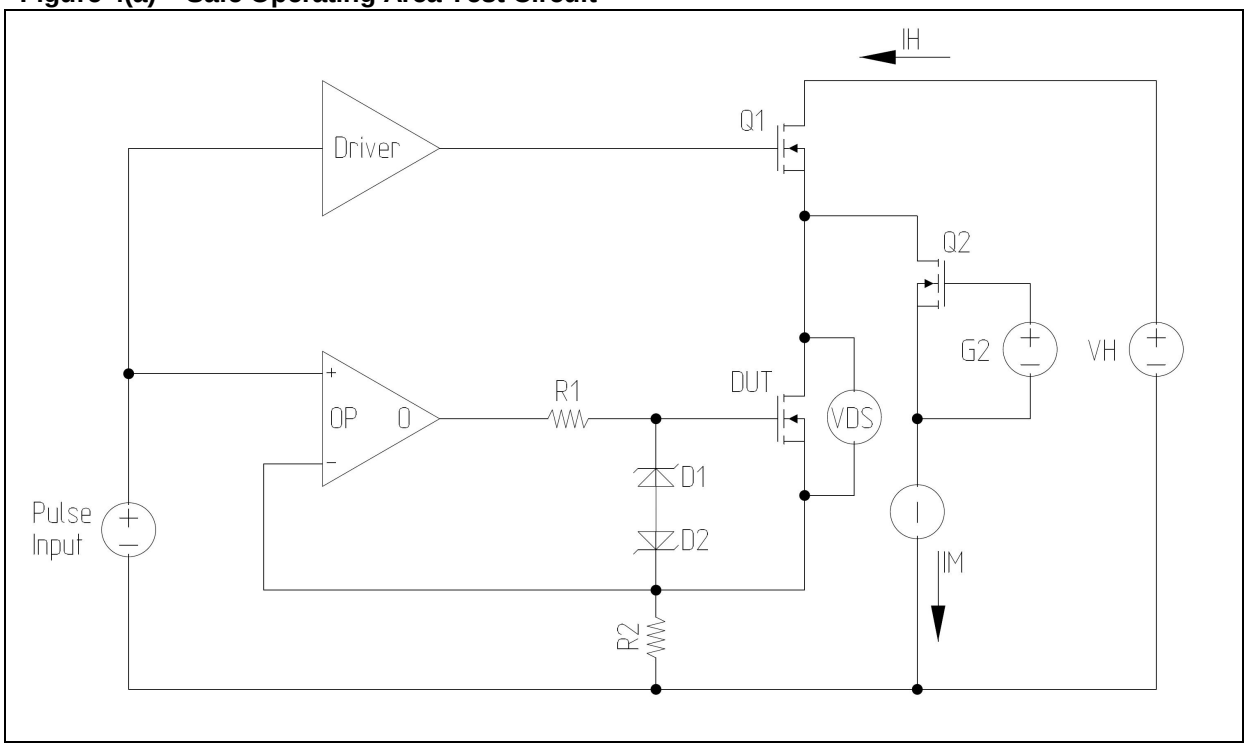
NOTES see Notes of table 2(a)

Table 3(b) – Electrical Measurements at Low Temperature (Ta = -55 °C -0 °C/+5 °C)

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS Variants 01,02,03	2	5	V

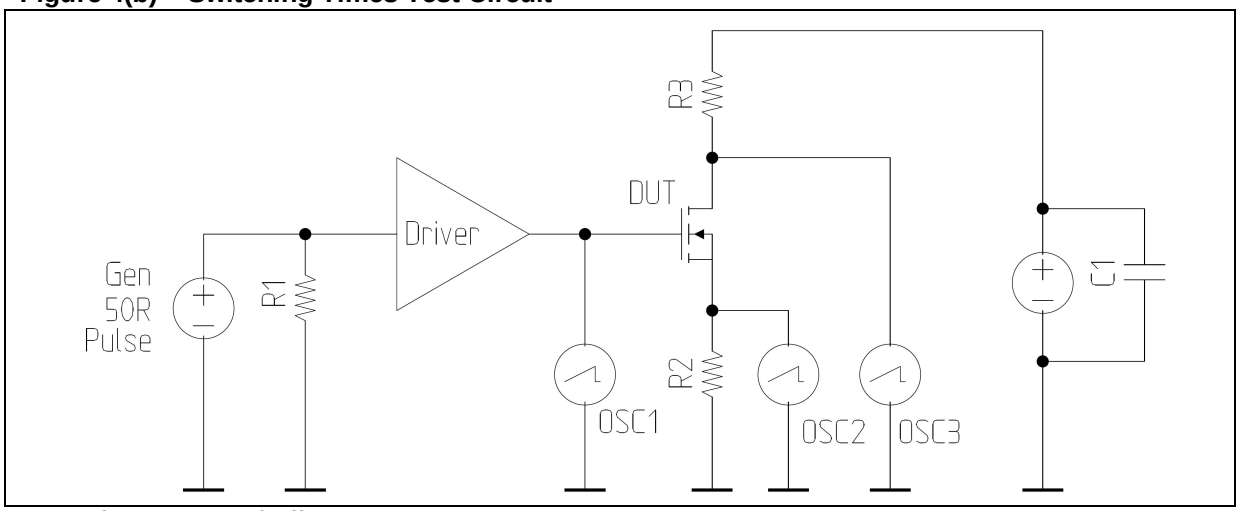
NOTES see Notes of table 2(a)

Figure 4 – Circuits for Electrical Measurements
Figure 4(a) – Safe Operating Area Test Circuit



IH = Heat Current; IM = Measurement Current; VH = Heat Voltage
Pulse Input: as specified in Paragraph 4.7.6

Figure 4(b) – Switching Times Test Circuit



C1: Voltage Source buffer
OSC1 – OSC3: Oscilloscope 1 – 3
OSC1: VGS(ON) and VGS(OFF), OSC3; VDS(ON) and VDS(OFF)
Pulse Input < 100 µs

Switching Time Test Signals

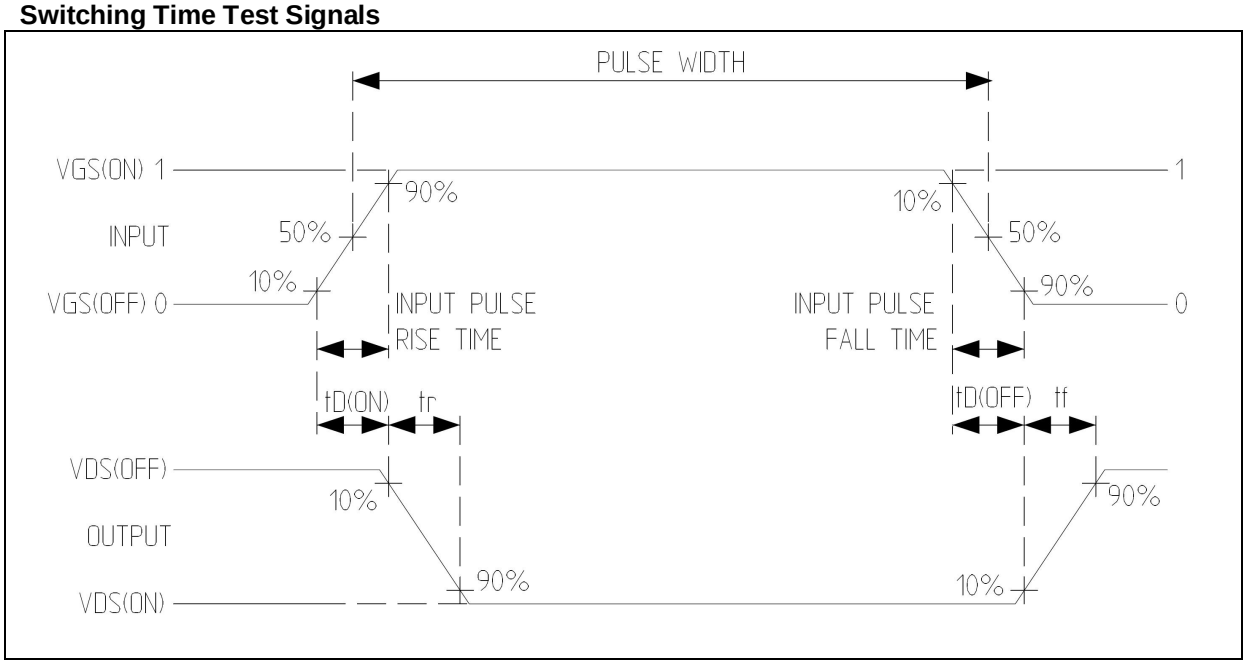


Table 4 – Parameter Drift Values

No.	Characteristics	Symbol	Spec. and/or Test Method	Test Conditions	Change Limits (Δ)	Unit
2	Gate Threshold Voltage	VGS(th)	As per table 2	As per table 2	-20 / 20	%
3	Forward Gate to Source Leakage Current	IGSSF	As per table 2	As per table 2	-20 / 20	nA
4	Reverse Gate to Source Leakage Current	IGSSR	As per table 2	As per table 2	-20 / 20	nA
5	Drain Current	IDSS	As per table 2	As per table 2	-25 / 25	µA
6	Drain Source On Resistance	rDS(ON)	As per table 2	As per table 2	-20 / 20	%

Table 5(a) – Conditions for High Temperature Reverse Bias (HTRB)

No.	Characteristics	Symbol	Conditions	Unit
1	Ambient Temperature	Tamb	+150 (+0 -15)	°C
2	Drain Source Voltage	VDS	80	V
3	Gate Source Voltage	VGS	0	V
4	Duration	t	168	h

Table 5(b) – Conditions for High Temperature Gate Bias (HTGB)

No.	Characteristics	Symbol	Conditions	Unit
1	Ambient Temperature	Tamb	+150 (+0 -15)	°C
2	Drain Source Voltage	VDS	0	V
3	Gate Source Voltage	VGS	16	V
4	Duration	t	48	h

Table 5(c) – Conditions for Operating Life Test (Note 1)

No.	Characteristics	Symbol	Conditions	Unit
1	Junction Temperature	TJ	+140 – +150	°C
2	Power Dissipation	PD	Variants 01, 02: min. 70 (Note 2)	W
			Variant 03: min. 90 (Note 2)	W
3	Duration	t	2000	H

Table 5(d) – Conditions for Intermittent Power Cycles

No.	Characteristics	Symbol	Conditions	Unit
1	Junction Temperature	TJ	+125 +15/-10	°C
2	Heating time	t(ON)	10	sec
3	Cycles		6000	
4	Drain Source Voltage	VDS	10	V
5	Drain Current	ID	Variant 01: min. 1.0 (Note 3)	A
			Variant 02: min. 0.4 (Note 3)	A
			Variant 03: min. 0.8 (Note 3)	A

NOTES:

1. Using the circuit in figure 5(c) and 5(d), power shall be applied to the device.
   Parts shall be thermally conductive mounted to a liquid cooled heat sink so that the specified junction temperature (TJ) will be reached.
   The junction temperature (TJ) should be determined by measurement of the reverse diode.
2. Power dissipation to be adjusted to the specified junction temperature (TJ)
3. Drain Current to be adjusted to the specified junction temperature (TJ)

Figure 5(a) – Electrical Circuit for High Temperature reverse Bias (HTRB) Burn In

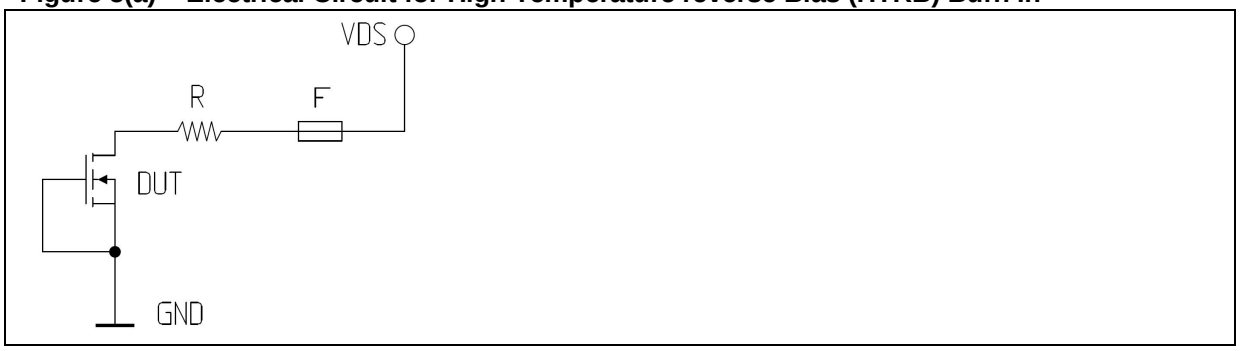


Figure 5(b) – Electrical Circuit for High Temperature Gate (HTGB) Burn In

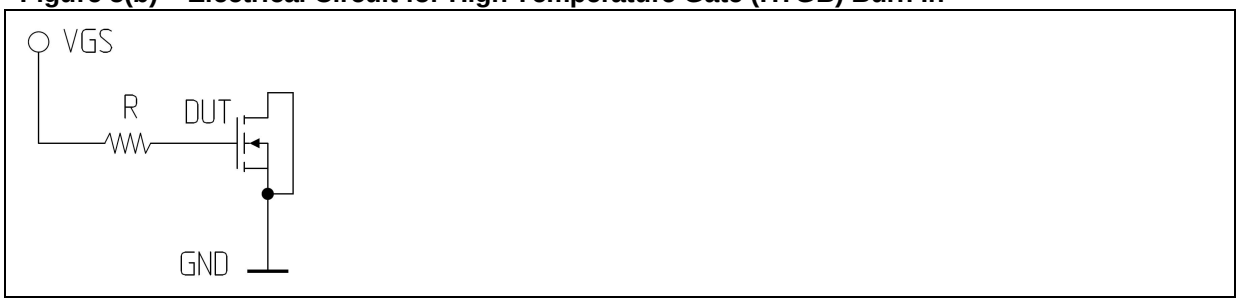


Figure 5(c) – Electrical Circuit for Operating Life Test

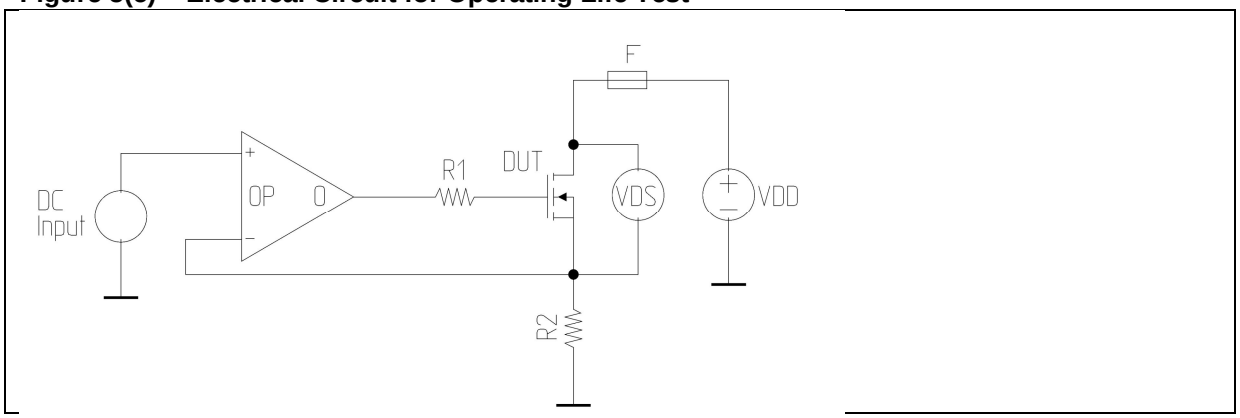
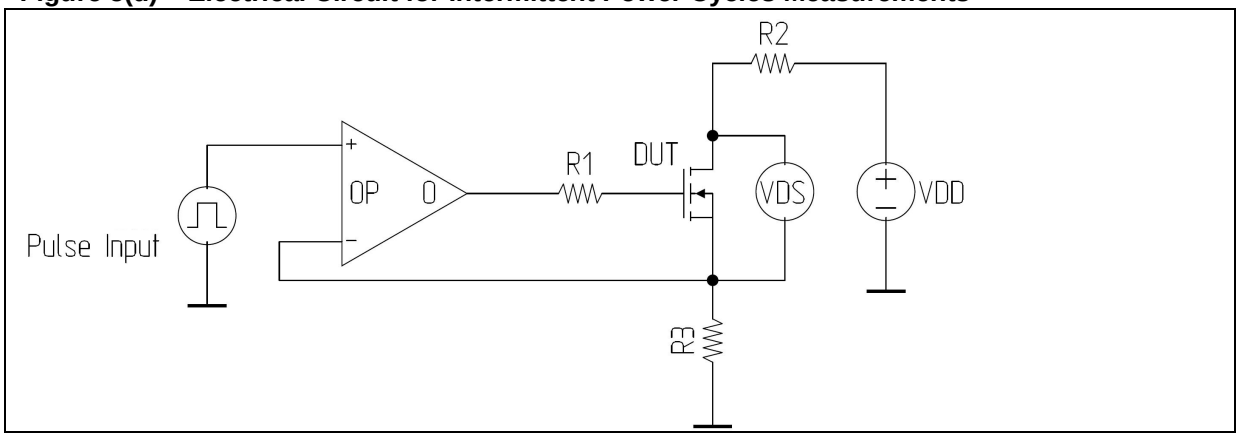


Figure 5(d) – Electrical Circuit for Intermittent Power Cycles Measurements



IH = Heat Current, VH = Heat Voltage

4.8 Environmental / Mechanical, Endurance Tests and Assembly and Capability Test (Chart F4 of DLR-RF-PS-STD-006)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are schedule in table 2 of this specification. Unless otherwise stated, the measurements shall be performed at Tamb = 25°C +/- 5°C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in table 6 of this specification. Unless otherwise stated, the measurements shall be performed at Tamb = 25 °C +/- 5 °C.

4.8.3 Electrical Circuit for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in figure 5(c) of this specification

4.8.4 Electrical Circuit for Intermittent Power Cycles Measurements

The circuit to be used for performing the intermittent measurements shall be the same as shown in figure 5(d) of this specification.

4.8.5 Conditions for Operating Life Tests

The requirements of operating life testing are specified in paragraph 8.19 of DLR Generic Specification no. DLR-RF-PS-STD-006 and amended of paragraph 4.2.3. The conditions for operating life testing shall be the same as specified in table 5(c) of this specification.

4.8.6 Conditions for Intermittent Power Cycles Measurements

The requirements for intermittent measurements are specified in MIL-STD-750 TM 1042, test condition ‘D’ and amended of paragraph 4.2.3. The condition shall be the same as specified in table 5(d) of this specification.

Table 6 – Parameter Electrical Measurements at Intermediate Points and on Completion of Endurance Testing

No.	Characteristics	Symbol	Spec. and/or Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
1	Gate Threshold Voltage	VGS(th)	As per table 2	As per table 2	2	4	V
2	Forward Gate to Source Leakage Currents	IGSS(F)	As per table 2	As per table 2	-	100	nA
3	Reverse Gate to Source Leakage Currents	IGSS(R)	As per table 2	As per table 2	-100	-	nA
4	Drain Current	IDSS	As per table 2	As per table 2	-	250	µA

4.9 Total Dose Irradiation Testing

4.9.1 Application

If specified in customer purchase order, total dose irradiation testing shall be performed in accordance with the requirements and test methods of ESCC Basic Specification No. 22900 Total Dose Steady – State Irradiation. Parts are divided into 2 Subgroups with same quantity for Gate Bias and Source Bias irradiation testing. As a minimum 5 samples for each Subgroup shall be tested.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in figure 6 of this specification.

Figure 6(a) – Bias Conditions for Irradiation Testing Gate Bias

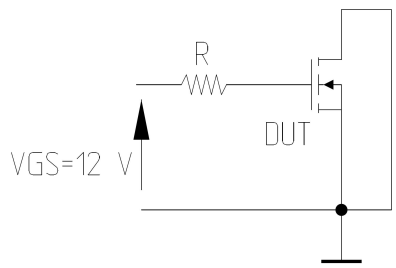
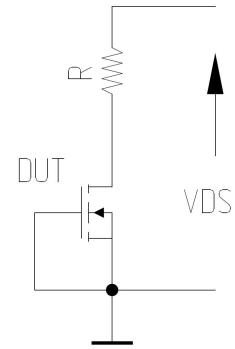


Figure 6(b) – Bias Conditions for Irradiation testing Source Bias



Source Bias Conditions: VDS = 80 V

Radiation Dose shall be increased sequentially by enlargement of the exposure time as defined in the table below. Radiation Dose Rate shall be Standard Rate 1-10 rad/s (3,6 – 36 krad/hr).

Irradiation Step	Radiation Dose after Irradiation Step [Rad(Si)]
1	3k
2	10k
3	20k
4	30k
5	50k
6	100k
7	300k

Electrical characteristics as listed in the table 7 shall be measured prior to exposure and within a maximum of 1h after each irradiation step. Control device parameters shall also be measured. A maximum time of 2h between consecutive exposures shall be observed. If a component exceeds the limits of the table below no further exposure shall take place and annealing cycles shall be performed.

Annealing Conditions:

- 1st annealing step: 25 °C anneal under bias for 168 hours, electrical characteristics shall be measured after 12, 24 and 168 hours.
- 2nd annealing step: Accelerated ageing under bias 168 hours at 100° C +/- 5% followed by an electrical measurement.

Table 7 – Electrical Measurements after completion of individual test steps and on Completion of Irradiation Testing

No.	Characteristics	Symbol	Spec. and/or Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
1	Breakdown Voltage Drain Source	BVDSS	As per table 2	As per table 2	100	-	V
2	Gate Threshold Voltage	VGS(th)	As per table 2	As per table 2	2	4	V
3	Forward Gate to Source Leakage Current	IGSSF	As per table 2	As per table 2	-	100	nA
4	Reverse Gate to Source Leakage Current	IGSSR	As per table 2	As per table 2	-100	-	nA
5	Drain Current	IDSS	As per table 2	As per table 2	-	250	µA
6	Drain Source On Resistance	RDS(ON)	As per table 2	As per table 2 Variant 01	-	0.04	Ω
				Variants 02, 03	-	0.03	Ω