Assembly and Test Houses:

Integrated Circuits, Monolithic,

Hermetically Sealed

Generic Specification No. 9200

Issue 1
Assembly and Test Houses:

Integrated Circuits, Monolithic,

Hermetically Sealed

Generic Specification No. 9200

Issue 1

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1. INTRODUCTION

1.1 SCOPE
This specification defines the general requirements for the capability approval, capability approval maintenance, procurement, and delivery of hermetically sealed Monolithic Integrated Circuit components for space applications packaged and tested at an Assembly and Test House (ATH). As described below two variants of the capability approval can be applied.
This specification contains the procurement of the Monolithic Integrated Circuit dice from the die manufacturer and the assembly of these dice into packages together with the appropriate inspection and test schedules and also specifies the data documentation requirements.

1.2 APPLICABILITY
This specification is primarily applicable to the granting of one of the following two capability approval variants to components assembled and tested in an ATH according to ESCC Basic Specification No. 24300 and to DLR No. 2439200 and the procurement of such components from capability approved ATH. It may also be applied for procurement of components assembled and tested at an ATH without capability approval.

ATH Product Capability Approval
The ATH Product Capability Approval of a component technology demands that all requirements for a component technology including the semiconductor chip technology are successful met as specified within this specification and the specification DLR No. 2439200. After successful completion of the capability approval program as given in this specification components within the specified capability domain are considered as qualified components.

ATH Capability Approval
The ATH Capability Approval requires the successful performance of all activities by the ATH for the assembly and testing of components as specified within this specification and the specification DLR No. 2439200. Components delivered by a ATH with a ATH Capability Approval can not be considered as qualified components. As long as these components are within the specified capability domain only the assembly and testing of the components can be considered as qualified.

2. APPLICABLE DOCUMENTS
The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on date of starting capability approval or placing the Purchase Order.

2.1 ESCC SPECIFICATIONS
- No. 20400, Internal Visual Inspection.
- No. 20500, External Visual Inspection.
- No. 20600, Preservation, Packaging and Dispatch of ESCC Electronic Components.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 21400, Scanning Electron Microscope Inspection of Semiconductor Dice.
- No. 21700, General Requirements for the Marking of ESCC Components.
- No. 22800, ESCC Non-conformance Control System.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23500, Lead Materials and Finishes for Components for Space Application.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.
For capability approval and capability approval maintenance or procurement of components, with the exception of ESCC Basic Specifications Nos. 21700, 22800, 24300, 24600, where ATH’s specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the DLR.

Such replacements shall be clearly identified in the applicable Process Identification Document (PID).

2.2 DLR SPECIFICATIONS
- No. 2439200 Assembly and Test Houses: Requirements for Capability Approval of Monolithic Microcircuit Technologies

2.3 OTHER (REFERENCE) DOCUMENTS
- ECSS-Q-70-02 Thermal Vacuum Outgassing Test for the Screening of Space Materials.

2.4 ORDER OF PRECEDENCE
For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:
(a) The Detail Specification.
(b) This Generic Specification.
(c) ESCC and DLR specifications.
(d) Other referenced specifications.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS
The terms, definitions, abbreviations, symbols and units specified in the ESCC Basic Specification No. 21300 shall apply. In addition following definitions apply:

ATH Assembly and Test House
DLR Deutsches Zentrum für Luft- und Raumfahrt
Assembly and Test House A company which procures the Monolithic Microcircuit Chips from the semiconductor manufacturer in the needed quality and at agreed standards, assembles these chips into packages and performs all relevant and required inspections, testings and measurements at chip and package level.
Semiconductor Manufacturer A company which designs the Monolithic Microcircuit Chips, develops the processes for the Chip Fabrication and performs the Chips Production in the required characteristic and quality.
Statistical Process Control (SPC) SPC utilises statistical methods to monitor parameters (i.e. process or product) in order to provide early warning of a process
fluctuation or shift. Appropriate actions must be taken to maintain a state of statistical control. SPC may be used as tool to facilitate process improvement.

4. **REQUIREMENTS**

4.1 **GENERAL**

The requirements for approval of capability domain and the qualification of a component (type approval testing) within an approved domain are given in this specification and the DLR Specification No. 2439200. Test samples submitted to the capability approval testing and the type approval testing shall have passed successful Special Assembly Controls, Wafer Lot Acceptance Test with Radiation Tests (if specified) and Screening Tests.

The test requirements for procurement of components shall comprise Special Assembly Controls, Wafer Lot Acceptance with Radiation Tests if required in the Purchase Order, Screening Tests, together with Periodic Tests for qualified components and Lot Validation testing for qualified (if required in the Purchase Order) and unqualified components (see Chart F1).

**Note:** Components from a source with an [ATH Capability Approval](#) only shall be considered as unqualified components.

4.1.1 **Specifications**

For capability approval, capability approval maintenance, procurement and delivery of components in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 **Conditions and Methods of Test**

The conditions and methods of test shall be in accordance with this specification, the ESCC and DLR Basic Specifications referenced herein and the Detail Specification.

4.1.3 **Assembly and Test House’s Responsibility for Performance of Tests and Inspections**

The ATH shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the ATH unless it is agreed by the DLR (for capability approval, capability approval maintenance, or procurement of qualified components) or the orderer (for procurement of unqualified components), to use an approved external facility.

4.1.4 **Inspection Rights**

The DLR (for capability approval and capability approval maintenance) or the orderer (for procurement of components) reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 **Pre-encapsulation Inspection Witnessing**

If required in the Purchase Order, the orderer may witness or perform the pre-encapsulation inspection and the ATH must notify the orderer at least 2 working weeks before the commencement of the inspection.
4.2 CAPABILITY APPROVAL AND CAPABILITY APPROVAL MAINTENANCE REQUIREMENTS ON A ASSEMBLY AND TEST HOUSE

To obtain and maintain the **ATH Product Capability Approval** or the **ATH Capability Approval** for a defined domain as described in Paragraph 1.2 of this specification, the ATH has to satisfy the requirements of ESCC Basic Specification No. 24300 and of the DLR specification No. 2439200.

4.3 DELIVERABLE COMPONENTS

Components delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID). Each delivered component shall be traceable to its assembly lot and its wafer lot. Components delivered to this specification shall have satisfactorily completed all the required tests.

Components delivered to this specification shall be produced from lots that are capable of passing all applicable tests, and sequences of tests, that are defined in Chart F4. The ATH shall not knowingly supply components that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a component is found to be in a condition such that it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

4.3.1 Lot Failure

Lot failure may occur during Special Assembly Controls (Chart F2), Wafer Lot Acceptance (Chart F2), Screening Tests (F3) or Capability Approval, Capability Approval Maintenance and Lot Validation Tests (Chart F4).

Should such failure occur during capability approval, capability approval maintenance or procurement of components coming from a source with **ATH Product Capability Approval** or with **ATH Capability Approval** the ATH shall initiate the non-conformance procedure in accordance with ESCC Basic Specification No. 22800. The ATH shall notify the orderer and the DLR by any appropriate written means within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing shall be performed on the failed components.

Should such failure occur during procurement of components from a source without a **ATH Product Capability Approval** or without a **ATH Capability Approval** the ATH shall notify the orderer by any appropriate written means within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing shall be performed on the failed components. The orderer shall inform the ATH within 5 working days of receipt of notification what action shall be taken.

4.4 MARKING

All components procured and delivered to this specification shall be marked in accordance with ESCC Basic Specification No. 21700. However, for components qualified under the **ATH Product Capability Approval** the “ESCC Qualified Components Symbol” has to be replaced by the “DLR Qualified Components Symbol”. Furthermore, for all components delivered under this specification the “ESCC Component number” shall be replaced by the “DLR Component number” as specified in the Detail Specification.
4.5 MATERIALS AND FINISHES

Specific requirements for materials and finishes are specified in the Detail Specification. Where a definite material and finish is not specified a material and finish shall be used so as to ensure that the component meets the performance requirements of this specification and the Detail Specification. Acceptance or approval of any constituent material and finish does not guarantee acceptance of the finished product.

Unless otherwise specified in the Detail Specification the component shall be hermetically sealed and shall have a metal body with hard glass seal or a ceramic body. The component case lid shall be welded, brazed, preform soldered or glass frit sealed.

All non-metallic materials and finishes, that are not within a hermetically sealed enclosure, of the components specified in the Detail Specification shall meet the requirements as outlined in ECSS-Q-70-02.

4.6 RADIATION TESTING

For capability approval or capability approval maintenance radiation testing shall be performed when specified in the Detail Specification to the total dose level given.

For procurement as required in the Purchase Order radiation testing shall be performed to the total dose level given in the Detail Specification or to an alternate level if so required in the Purchase Order.

The capability approval status of the procured components shall not be impacted by any change to the total dose level applied.

For procurement any lot of components that fails the required total dose radiation test level may be accepted to a lower level of radiation subject to satisfactory test results at the lower level. In this case the total dose radiation level identification letter for the lot shall be modified accordingly.

4.7 PROCUREMENT OF MONOLITHIC MICROCIRCUIT WAFERS/DICE

4.7.1 General

The procurement of Monolithic Microcircuit wafers/dice by the ATH from the semiconductor manufacturer shall comprise the following requirements:

- For the ATH Product Capability Approval the wafers/dice have to meet all requirements as specified in the specification DLR 2439200. Furthermore, all definitions, data and documentation requirements of DLR 2439200 have to be defined in the capability domain description, the PID and/or delivered with the wafers/dice from the semiconductor manufacturer.

- For the ATH Capability Approval the wafers/dice procurement have to meet those criteria which are defined in the domain description for this variant (see DLR 2439200). Furthermore, all definitions, data and documentation requirements of this variant as defined in DLR 2439200 have to be delivered with the wafers/dice from the semiconductor manufacturer.

- For sources without a capability approval the wafer/die procurement has to be made from semiconductor manufacturers which have to ensure that all test and inspection requirements of this specification can be met by the semiconductor and that the applied processes at the ATH will not degrade the semiconductor chip performance.
4.7.2 **Supplier Selection**

The ATH shall assure that the selected supplier of the Monolithic Microcircuit wafers/dice provides all information necessary to comply with the requirements of the applicable variants as defined in Paragraph 4.7.1 above.

4.7.3 **Selection of Monolithic Microcircuit Dice**

For the **ATH Product Capability Approval** and the **ATH Capability Approval** the Monolithic Microcircuit die shall be selected in accordance to the requirements of specification DLR No.2439200, this specification and the applicable detail specification. For sources without capability approval the requirements of this specification and the applicable detail specification have to be met.

It is the ATH's responsibility to demonstrate that the selected Monolithic Microcircuit die is:
- suitable for the mounting and testing process used,
- reliable in the component's environment,
- meeting the specification requirements.

4.7.4 **Procurement Specifications for Monolithic Microcircuit Dice**

For procurement and delivery of Monolithic Microcircuit dice in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

The semiconductor dice shall be controlled via a procurement specification. Where available, existing ESCC detail specifications or MIL-specifications shall be used.

These procurement specifications shall be:
(a) compliant with one of the existing standardisation systems,
(b) approved by the DLR (Capability Approval) or the orderer (ordered flight parts),
(c) subject to configuration control,
(d) mentioned in the PID.

The procurement specifications for Monolithic Microcircuit dice shall as a minimum define:
(a) supplier's name,
(b) location of foundry,
(c) revision of chip design (if applicable),
(d) capability approval program (if applicable)
(e) lot definition,
(f) maximum ratings,
(g) applicable die attach and bonding parameter,
(h) electrical parameters,
(i) chip layout and size,
(j) backside and front metalisation system and requested passivation,
(k) required tests and inspection at semiconductor manufacturer,
(l) radiation requirements (if applicable),
(m) requested quality level and/or inspection criteria,
(n) traceability requirements,
(o) packaging requirements,
(p) data to be supplied,
(q) the delivery conditions.

4.7.5 **Conditions and Methods**

The test methods and conditions which are applied at the semiconductor manufacturer for the testing and selection of the chips have to be defined in the die procurement specification and in addition for the **ATH Product Capability Approval Program** in the PID of the semiconductor manufacturer.
The test methods and conditions applied at chip level by the ATH for incoming inspection and/or for the preparation of the assembly process have to be defined in the incoming inspection procedure respectively in the applicable PID.

4.7.6 Production Lot

All semiconductor wafers/dice shall be procured as traceable homogeneous lots.

- a homogeneous lot is defined as dice from a unique wafer or wafer lot with respect to same design, identical materials from the same material charge, performed by the same diffusion, metalisation and passivation processes and fabricated on the same production line by the same personnel in a limit time period.

Each lot is assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the manufacturing process.

4.7.7 Traceability

All Monolithic Microcircuit dice used shall be traceable to their wafer lot and the applied incoming inspection process.

Records shall be maintained to provide traceability from the specific wafer lot to the assembled component lot.

4.7.8 Control of Changes

The ATH is responsible for controlling all changes at die level. The changes must be evaluated by the ATH for impact on the reliability and performance of the component. Any change has to be documented. Additional needed or deleted testing of components due to changes must be also recorded. Furthermore, the control of changes shall also include obsolescence and future availability of the semiconductor dice. Changes have to be reported to the DLR for the ATH Product Capability Program and ATH Capability Program and to the orderer for procurement.

4.7.9 Incoming Inspection

Each received wafer/die lot at the ATH shall be submitted to an incoming inspection process. This process shall verify characteristics such as:

(a) conformance with the procurement conditions,
(b) lot homogeneity,
(c) conformance with required visual criteria,
(e) compliance of test data and documentation with requirements.

As part of the incoming inspection on sample base the die attach and the bondability of the received lot shall be tested at the ATH as follows:

- Sample size: 2 or 3 dice
- Mounting process: Each die shall be mounted to the package and bonded with the same materials and processes as it is defined in the PID for the assembly process of the complete received lot. The bonds and the die attach have to meet the visual inspection criteria as defined in the ESCC Basic specification No. 20400. A single failure shall be cause for rejection of the delivered die lot.
- Bond strength: MIL-STD-883 Test Method 2011,
- Test condition C or D for thermo-compression, ultrasonic or wedge bonding.
- Test condition F for flip-chip bonding.
Quantity of bond wires 8 or less; Test samples = 3, Test all bonds
Quantity of bond wires 9 to 24; Test samples = 2, Test all bonds
Quantity of bond wires 25 or more; Test samples = 2, Test 50% of bonds.
Individual separation force and categories shall be recorded.
A single failure shall be cause for rejection of the delivered die lot.

Individual separation force and categories shall be recorded.
A single failure shall be cause for rejection of the delivered die lot.

4.7.10 Handling and Storage of Monolithic Microcircuit dice
The ATH shall have a specification in place which defines the appropriate requirements and give sufficient guidelines and support for handling and storage of Monolithic Microcircuit wafers/dice suitable for space application.

4.7.11 Documentation
Documentation requirements for die procurement and incoming inspection of the wafers/dice shall be in accordance with Para. 9.6 of this specification.

5. PRODUCTION CONTROL

5.1 GENERAL
The minimum requirements for production control shall be defined in the Process Identification Document (PID).

Unless otherwise specified in the Detail Specification all lots of components used for Capability and Capability Maintenance, Lot Validation Testing and for delivery shall be subjected to tests and inspections in accordance with Chart F2.

Any components which do not meet these requirements shall be removed from the lot and at no future time resubmitted to the requirements of this specification.

The applicable test requirements are detailed in the paragraphs referenced in Chart F2.

In case of lot failure, the ATH shall act in accordance with Para. 4.3.1.

5.1.1 Rebonding
The rebonding of wires during assembly is not permitted.
5.2

 AFER LOT ACCEPTANCE

5.2.1 Process Monitoring Review
For the ATH Product Capability Approval Program wafer process monitoring has to be performed in accordance with the semiconductor manufacturer’s SPC program as defined in the semiconductor manufacturer’s PID. A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID.

5.2.2 Scanning Electron Microscope (SEM) Inspection
Components supplied to this specification shall be produced from wafer lots that have been subjected to, and successfully met the Scanning Electron Microscope Inspection requirements in accordance with Para. 8.3.
If the Scanning Electron Microscope Inspection will not be performed by or under the responsibility of the semiconductor manufacturer, ATH has related to a wafer or a wafer lot to perform itself or to order at an external source the Scanning Electron Microscope Inspection.

5.2.3 Total Dose Radiation Testing
For capability and capability maintenance:
- If specified in the Detail Specification, components shall be produced from a wafer lot which has been subjected to and successfully completed total dose radiation testing in accordance with Para. 8.4 to the total dose level given.

During procurement:
- If specified in the Detail Specification and required in the Purchase Order, components shall be produced from a wafer lot which has been subjected to and successfully completed total dose radiation testing in accordance with Para. 8.4 to the required total dose level.

If the Total Dose Radiation Testing will not be performed by or under the responsibility of the semiconductor manufacturer, ATH has related to a wafer or a wafer lot to order the radiation testing at an external source.

5.2.4 Documentation
Documentation of Wafer Lot Acceptance shall be in accordance with Para. 9.7

5.3 SPECIAL ASSEMBLY CONTROLS

5.3.1 Process Monitoring Review
Assembly Process monitoring review shall be done in compliance with the ATH’s SPC rules described in the PID. The assembly lot shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID.
5.3.2 Pre-encapsulation Inspection

Pre-encapsulation inspection shall consist of internal visual inspection in accordance with Para. 8.1 and bond strength and die shear test in accordance with Para. 8.2.

Bond Strength and die shear tests shall be performed on test samples in accordance with Para. 8.2. A single failure shall cause for lot failure. These tests are considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.3 Dimension Check

In accordance with Para. 8.10 on 3 samples only.

If a failure occurs, the complete lot shall be checked.

5.3.4 Weight

The maximum weight of the components specified in the Detail Specification shall be guaranteed but not tested.

5.3.5 Documentation

Documentation of Special Assembly Controls shall be in accordance with Para. 9.5.

6. SCREENING TESTS

6.1 GENERAL

Unless otherwise specified in the Detail Specification, all components used for Capability Approval and Capability Approval Maintenance, Lot Validation Testing, and for delivery, shall be subjected to tests and inspections in accordance with Chart F3. All components shall be serialised prior to the tests and inspections.

Unless otherwise specified in the Detail Specification, the tests shall be performed in the order shown.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test methods and conditions are specified in the paragraphs referenced in Chart F3.
6.2 FAILURE CRITERIA

6.2.1 Environmental and Mechanical Test Failure
The following shall be counted as component failures:
- components which fail during tests for which the pass / fail criteria are inherent in the test method, i.e. PIND, solderability, seal.

6.2.2 Parameter Drift Limits
The acceptable change limits are shown in the Parameter Drift Values in the Detail Specification. A component shall be counted as a parameter drift failure if the changes during high temperature reverse bias burn-in or during power burn-in are larger than the drift values (Δ) specified.

6.2.3 Parameter Limit Failure
A component shall be counted as a limit failure if one or more parameters exceed the limits given in Electrical Measurements at Room, High and Low Temperatures in the Detail Specification.

Any component which exhibits a limit failure prior to the submission to HTRB burn-in shall be rejected and not counted when determining lot rejection.

6.2.4 Other Failures
A component shall be counted as a failure in any of the following cases:
- External Visual Inspection failure.
- Mechanical failure.
- Handling failure.
- Lost component.

6.3 Failed Components
A component shall be considered as a failed component if it exhibits one or more of the failure modes described in Para. 6.2.

6.4 LOT FAILURE
In the case of lot failure, the ATH shall act in accordance with Para. 4.3.1.

6.4.1 Lot Failure during 100% Testing
If the number of components failed on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3 exceeds 5% (rounded upwards to the nearest whole number) of the components submitted to initial measurements of Parameter Drift Values of Chart F3, the lot shall be considered as failed.
If a lot is composed of groups of components of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

6.4.2 Lot Failure during Sample Testing

A lot shall be considered as failed if the number of allowable failures during sample testing as specified in the Detail Specification, is exceeded.

If a lot failure occurs, 100% testing may be performed but the cumulative percentage defective shall not exceed that given in Para. 6.4.1.

No failures are allowed for the solderability test.

6.5 DOCUMENTATION

Documentation of Screening Tests shall be in accordance with Para. 9.8.

7. CAPABILITY APPROVAL, CAPABILITY APPROVAL MAINTENANCE AND LOT VALIDATION TESTING

The requirements of this paragraph are applicable to the tests performed for qualification and qualification maintenance of components within a capability approved domain and also for lot validation testing.

7.1 CAPABILITY APPROVAL (QUALIFICATION) FOR A DEFINED DOMAIN

7.1.1 General

Capability Approval testing shall be in accordance with the requirements given in Chart F4. The tests of Chart F4 shall be performed on the specified sample, chosen at random from components which have successfully passed the tests in Chart F3 (screening tests). This sample constitutes the Capability Approval test lot.

The Capability Approval test lot is divided into subgroups of tests and all components assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Chart F4.

The conditions governing Capability Approval testing are given in ESCC Basic Specification No. 24300.

7.1.2 Distribution within the Capability Approval Test Lot

The capability domain as described in the specification DLR No. 2439200 covers ranges of components that are similar structured. The test lot shall be comprised of test structures as described in the specification DLR No. 2439200 or component types so selected that they adequately represent all of the various mechanical, structural and electrical peculiarities of that range. The designed test structures or the selected components shall be those that employ the
extremes of design rules and tolerances and contain the maximum of internal sub-circuitry complexity, i.e. usually those that give the greatest risk of rejection.

The distribution shall be as specified by, or agreed with, the DLR.

7.2
CAPABILITY APPROVAL MAINTENANCE (PERIODIC TESTING)

Capability Approval for the specified domain is maintained through periodic testing and the test requirements of Para. 7.1 shall apply. For each subgroup the period between successive subgroup testing shall be as given in Chart F4. The conditions governing capability approval maintenance are given in ESCC Basic Specification No. 24300.

7.3
COMPONENT TYPE APPROVAL TEST

A component type which is defined by an appropriate Detail Specification and is manufactured within an approved Product Capability domain or an approved Capability domain by an approved ATH has to pass successful a Component Type Approval Test, if in the frame of the Capability Approval no samples from this part type have been successful submitted to Chart F4, Subgroup 2 as specified in Para. 8.19 of this specification.

The Component Type Approval Test shall constitute those tests defined in the DLR Basic Specification No. 2439200.

7.4
LOT VALIDATION TESTING

7.4.1
General

For qualified components within approved Product Capability domain, Lot Validation Testing as described in Chart F4, Subgroup 2, shall only be performed on the procured lot if required in the Purchase Order.

If unqualified components are procured using this specification then the Orderer shall define in the Purchase Order the required subgroups from Chart F4 to be used for Lot Validation Testing.

7.4.2
Distribution within the Sample for Lot Validation Testing

Where the Detail Specification covers a range, or series, of components that are considered similar, then it is only necessary to perform Lot Validation Testing on representative types if a number of different types are procured together. The sample for Lot Validation Testing shall be comprised of component types so selected that they adequately represent all of the various mechanical, structural and electrical peculiarities of the component procured from the range or series.

The distribution of component types will vary from procurement to procurement and shall be as required in the Purchase Order.

7.5
FAILURE CRITERIA

The following criteria shall apply to Capability Approval, Capability Approval Maintenance and Lot Validation Testing.
7.5.1 Environmental and Mechanical Test Failures

The following shall be counted as component failures:

- Components which fail during tests for which the pass / fail criteria are inherent in the test method, e.g. seal, terminal strength, etc.

7.5.2 Electrical Failures

The following shall be counted as component failures:

- Components which fail one or more of the applicable limits and/or drift values (when specified) at each of the relevant data points specified for environmental, mechanical and endurance testing in intermediate and End-Point Electrical Measurements in the Detail Specification.

7.5.3 Other Failures

A component shall be counted as a failure in any of the following cases:

- Visual Inspection failure
- Mechanical failure
- Handling failure
- Lost component

7.6 FAILED COMPONENTS

A component shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 7.5.

When requested by the DLR (for capability approval, capability approval maintenance or procurement of qualified components) or the Orderer (for procurement of qualified or unqualified components), failure analysis of failed components shall be performed by the ATH and the results provided.

Failed components shall be retained at the ATH’s plant until the final disposition has been agreed and certified.

7.7 LOT FAILURE

For capability approval and capability approval maintenance, the lot shall be considered as failed if one component in any subgroup of Chart F4 is failed based on the criteria given in Para. 7.5.

For procurement, the lot shall be considered as failed if one component in any test specified for Lot Validation testing is failed based on the criteria given in Para. 7.5.

In the case of lot failure, the ATH shall act in accordance with Para. 4.3.1.
7.8 CAPABILITY APPROVAL, CAPABILITY APPROVAL MAINTENANCE AND LOT VALIDATION TESTING SAMPLES

All tests of Chart F4 are considered to be destructive and therefore components so tested shall not form part of the delivery lot.

7.9 DOCUMENTATION

Documentation of Capability Approval, Capability Approval Maintenance and Lot Validation Testing shall be in accordance with Para. 9.9.

8. TEST METHODS AND PROCEDURES

If an ATH elects to eliminate or modify a test method or procedure, the ATH is still responsible for delivering components that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

For a qualified domain, documentation supporting the change shall be approved by the DLR and retained by the ATH. It shall be copied, when requested, to the DLR. The change shall be specified in an appendix to the Detail Specification and in the PID.

For components without any capability approval the change shall be approved by the Orderer. The change may be specified in an appendix to the Detail Specification at the request of the ATH or the Orderer.

8.1 INTERNAL VISUAL INSPECTION

ESCC Basic Specification No. 20400.

8.2 BOND STRENGTH AND DIE SHEAR TEST

8.2.1 Bond Strength

Test Method:
MIL-STD-883 Test Method 2011,
- Test Condition ‘C’ or ‘D’ for thermo-compression, ultrasonic or wedge bonding.
- Test condition ‘F’ for flip-chip bonding.

Test samples: For Special Assembly Controls the required test samples shall be selected at random from the lot of components accepted after internal visual inspection.

For Capability Approval and Capability Approval Maintenance tests the required test samples shall be selected from the components in Subgroup 3 of Chart F4.

Quantity of internal bond wires 8 or less; Test samples = 3, Test all bonds
Quantity of internal bond wires 9 to 24; Test samples = 2, Test all bonds
Quantity of internal bond wires 25 or more; Test samples 50% of bonds.
If agreed by the DLR (for Capability Approval or Capability Approval Maintenance) or the Orderer (for procurement) the test samples for Special Assembly Controls may have only passed the low magnification phase of the internal visual inspection.

Individual separation force and categories shall be recorded. A single failure shall be cause for lot failure.

8.2.2

Die Shear

MIL-STD-883 Test Method 2019

The same test samples submitted to bond strength shall be used. Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.3

SCANNING ELECTRON MICROSCOPE INSPECTION

ESCC Basic Specification No. 21400.

8.4

TOTAL DOSE RADIATION TESTING

ESCC Basic Specification No. 22900 to the total dose level specified in the Detail Specification or as required in the Purchase Order.

8.5

HIGH TEMPERATURE STABILISATION BAKE

MIL-STD-883, Test Method 1008, Duration: 24 hours at maximum storage temperature rating specified in the Detail Specification.

8.6

TEMPERATURE CYCLING

MIL-STD-883, Test Method 1010, Test Condition C.

8.7

PARTICLE IMPACT NOISE DETECTION (PIND)

Only applicable to components with cavities.

MIL-STD-883, Test Method 2020, Test Condition A.
8.8 SEAL

8.8.1 Seal, Fine Leak
MIL-STD-883, Test Method 1014, Test Condition A or B.

8.8.2 Seal, Gross Leak
MIL-STD-883, Test Method 1014, Condition C.

8.9 ELECTRICAL MEASUREMENTS

8.9.1 Parameter Drift Values
At each of the relevant data points during screening tests, parameter drift values shall be measured as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

8.9.2 High and Low Temperatures Electrical Measurements
High and low temperature electrical measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.9.3 Room Temperature Electrical Measurements
Room temperature electrical measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.9.4 Intermediate and End-Point Electrical Measurements
At each of the relevant data points during capability approval, capability approval maintenance and lot validation tests intermediate and end-point electrical measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if specified.

8.10 EXTERNAL VISUAL INSPECTION AND DIMENSION CHECK
External visual inspection shall be performed in accordance with ESCC Basic Specification No. 20500.

Dimension check (during special assembly controls only) shall be performed in accordance with ESCC Basic Specification No. 20500 and the Detail Specification on a sample of 3 components. If a failure occurs the complete lot shall be checked.

8.11 MECHANICAL SHOCK
8.12 VIBRATION

8.13 CONSTANT ACCELERATION
MIL-STD-883, Test Method 2001, Test Condition E (resultant centrifugal acceleration to be in the Y1 axis only). For components which have a package weight of 5 grammes or more, or whose inner seal or cavity perimeter is more than 5 cm, Condition D shall be used.

8.14 THERMAL SHOCK
MIL-STD-883, Test Method 1011. Test Condition C.

8.15 MOISTURE RESISTANCE

8.16 SOLDERABILITY
5 samples. A single failure shall be cause for lot failure.
MIL-STD-883, Test Method 2003, to be performed on all terminals.

Solderability testing may be performed on empty packages or electrical rejects. The test samples used must be of the same package type and must have been manufactured using the same process, at the same time and have been subjected to the same screening as the packages of the delivery lot with which they are associated.

For components with gold plated lead finish, activated fluxes (RMA and RA) may be used but shall be immediately cleaned off after dipping using an acceptable solvent.

Solderability testing is classed as destructive and therefore components so tested shall not form part of the delivery lot.

8.17 PERMANENCE OF MARKING
ESCC Basic Specification No. 24800.

8.18 TERMINAL STRENGTH
MIL-STD-883, Test Method 2004, Test Condition D for chip carrier packages or Test Condition B2 for all other packages. For Condition B2, 3 leads (excluding corner leads) or 10% of the leads (whichever is greater) shall be randomly selected on each component.

8.19 OPERATING LIFE
MIL-STD-883, Test Method 1005
- Duration: 2000 hours.
- Conditions: As specified in Operating Life in the Detail Specification.
- Data Points:
  As specified in Intermediate and End-point Electrical Measurements in the Detail Specification at 0 hours, 1000 ± 48 hours and 2000 ± 48 hours. If drift values are specified, the drift shall always be related to the 0-hour measurement.

8.20
HIGH TEMPERATURE REVERSE BIAS BURN-IN
MIL-STD-883, Test Method 1015, Test Condition A.
- Duration and Test Conditions
  As specified, where applicable, in High Temperature Reverse Bias Burn-In in the Detail Specification.
- Data Points
  As specified in the Parameter Drift Values in the Detail Specification at 0 hours and T (+24-0) hours (where T is the specified duration).

8.21
POWER BURN-IN
MIL-STD-883, Test Method 1015, condition B, D or E.
- Duration
  Unless otherwise specified in the Detail Specification, components shall be subjected to a total power burn-in period of 240 (+24 –0) hours.
- Test Conditions
  As specified in Power Burn-in in the Detail Specification. The alternative temperature and time combinations per MIL-STD-883 method 1015 are permissible provided that the maximum operating ratings for a component are not exceeded.
- Data Points
  As specified in the Parameter Drift Values in the Detail Specification at T (+24 -0) hours (where T is the specified duration).

If high temperature reverse bias burn-in is not being performed, the 0 hours (initial) measurement is also required.

9.
DATA DOCUMENTATION

9.1
GENERAL

For the capability approval, capability approval maintenance, lot validation and procurement for each lot a data documentation package shall exist in printed or electronic form.
This package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Special Assembly Controls data (Chart F2).
(e) Wafer Lot Acceptance (Chart F2).
(f) Screening Test data (Chart F3).
(g) Capability Approval and Capability Approval Maintenance Tests data including Lot Validation Testing data (when applicable) (Chart F4).
(h) Failed components list and failure analysis report (when applicable).
(i) Certificate of Conformity.

Items (a) to (i) inclusive shall be grouped, preferably as sub-packages and, for identification purposes, each page shall include the following information.

- DLR Component Number.
- ATH’s name.
- Lot identification.
- Date of establishment of the document.
- Page number.

Whenever possible, documentation should preferably be supplied in electronic format suitable for reading using a compatible PC. The format supplied shall be legible, durable and indexed. The preferred storage media are 3 ½ inch diskettes or CD-ROMS and the preferred file formats are ASCII or PDF.

9.1.1 Capability Approval and Capability Approval Maintenance

In the case of Capability Approval or Capability Approval Maintenance, the items listed in Para. 9.1(a) to (i) are required.

9.1.2 Component Procurement and Delivery

For all deliveries of components procured to this specification, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity)
(b) Certificate of Conformity (including range of delivered serial numbers)

9.1.3 Additional Documentation

The ATH shall deliver additional documentation containing data and reports to the Orderer, if required in the Purchase Order.
9.1.4
Data Retention / Data Access
If not delivered, all data shall be retained by the ATH for a minimum of 5 years during which time it shall be available for review, if requested, by the Orderer or the DLR (for capability approved components).

9.2
COVER SHEET(S)
The cover sheet(s) of the data documentation package shall include as a minimum:
(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable Generic Specification, including issue and date.
(c) DLR Component Number and the ATHs part type number.
(d) Lot identification.
(e) Range of delivered serial numbers.
(f) Number of the purchase order.
(g) Radiation testing level (if applicable).
(h) Information relative to any additions to this specification and / or the Detail Specification.
(i) ATH’s name and address.
(j) Location of the assembly and testing plant.
(k) Name and address of the semiconductor chip manufacturer.
(l) Location of the chip fabrication plant.
(m) Signature on behalf on ATH.
(n) Total number of pages of the data package.

9.3
LIST OF EQUIPMENT USED
A list of equipment used for tests and measurements shall be prepared, if not in accordance with the data given in the PID. Where applicable, this list shall contain inventory number, ATH’s type number, serial number, etc. This list shall indicate for which tests such equipment was used.

9.4
LIST OF TEST REFERENCES
This list shall include all ATH’s references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

9.5
SPECIAL ASSEMBLY CONTROL DATA (CHART F2)
A test result summary shall be compiled, showing the total number of components submitted to, and the total number rejected after each of the tests. For the bond-strength and die-shear tests, the separation forces and categories shall be recorded.
9.6
DIE PROCUREMENT AND INSPECTION DATA

A summary of the results of die procurement and inspection (with reference to the traceability information) shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Test data.
(e) Certificate of Conformity.

Each page shall include the following information.
- Die Number.
- Supplier’s name.
- Lot identification.
- Date of establishment of the document.
- Page number.

9.7
WAFER LOT ACCEPTANCE (CHART F2)

Data of SEM inspection shall be prepared in accordance with the requirements of ESCC Basic Specification No. 21400.

Radiation test report shall be prepared in accordance with the requirements of ESCC Basic Specification No. 22900 (if specified).

9.8
SCREENING TESTS DATA (CHART F3)

A test result summary shall be compiled showing the total number of components submitted to and the total number rejected after each of the tests. For each test requiring electrical measurements the results shall be recorded against component serial number. Component drift calculations shall be recorded for each specified test against component serial number.

9.9
CAPABILITY APPROVAL AND CAPABILITY APPROVAL MAINTENANCE DATA (CHART F4)

9.9.1
Capability Approval Tests

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against the component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against the component serial number.

9.9.2
Periodic Tests for Capability Approval Maintenance

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against
component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against the component serial number.

In addition to the full test data a report shall be compiled for each subgroup of Chart F4 to act as the most recent periodic testing summary. These reports shall include a list of all tests performed in each subgroup, the component numbers and quantity of components tested, a statement confirming all results were satisfactory, the date the tests were performed and a reference to the full test data.

9.9.3 Lot Validation Testing
For lot validation testing a test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup (as applicable). Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against the component serial number.

9.10 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT
The failed components list and failure analysis report shall provide full details of:

(a) The reference and description of the test or measurement performed as defined in this specification and/or Detail Specification during Special Assembly Controls, Wafer Lot Acceptance, Screening Tests and Capability Approval and Capability Approval Maintenance Tests.

(b) The serial number (if applicable) of the failed component.

(c) The failed parameter and the failure mode of the component.

(d) Detailed failure analysis (if requested by the DLR or Orderer).

9.11 CERTIFICATE OF CONFORMITY
A Certificate of Conformity shall be established as defined in the ESCC Basic Specification No 24300.

10. DELIVERY
For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.

(b) The components used for lot validation testing (when applicable), but not forming part of the delivery lot.

(c) The relevant documentation in accordance with the requirements of Section 9.

In the case of a component for which a valid capability approval and component type approval is in force, all data of all components submitted to lot validation testing shall also copied, when requested, to the DLR.
For capability approval or capability approval maintenance, the disposition of the test lot and its related documentation shall be as specified in ESCC Basic Specification Nos. 24300 and the relevant paragraphs of Section 9 of this specification.

11. **PACKAGING AND DISPATCH**

The packaging and dispatch of components to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 20600.
12. CHARTS

12.1 CHART F1: GENERAL FLOW FOR PROCUREMENT

Die Procurement and Inspection
- Wafer Lot Accept., Para. 5.2; Chart F 2
- Die Procurement, Para. 4.7
- Incoming Inspection, Para. 4.7.9

Special Assembly Control (Chart F2)
- Process Monitoring Review, Para. 5.3.1
- Pre-encapsulation Inspect., Para. 5.3.2
- Dimension Check, Para. 5.3.3
- Weight, Para. 5.3.4

Screening Tests, Para. 6; (Chart F 3)

Product Capability Approved Domain
- Lot Validation Testing (1 )
  Para 7.4.1 / Chart F4 Subgroup 2

Capability Approved Domain and Non Capability Approved Domain
- Lot Validation Testing
  Para. 7.4 / Chart F4

Deliverable Components

Release

Capability Approval Maintenance
(Periodic Testing)
Para. 7.2 / Chart F4

Delivery

NOTES:
1. Lot Validation Testing is optional for components from the Product Capability Approved Domain and shall only be performed if required in the Purchase Order.
12.2 CHART F2: PRODUCTION CONTROL

WAFER LOT ACCEPTANCE AND CHIP ASSEMBLY INTO THE PACKAGE

WAFER LOT ACCEPTANCE

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TO CHART F3 – SCREENING

Notes:
1) Performed on a sample basis.
2) Guaranteed but not tested.
3) If specified in the Detail Specification and required in the Purchase Order (for procurement).
## CHART F3: SCREENING TESTS

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**Notes:** see next page
Notes:
1. All components shall be serialised prior to Screening Tests.
2. The lot failure criteria of Para 6.4 shall apply to this test.
3. For Components with hot solder dip final lead finish the hot solder dip processing shall be performed at any time prior to Room Temperature Electrical Measurements during Screening Tests. The requirements for hot solder dip are specified in ESCC Basic Specification No. 23500.
4. Measurements of Parameter Drift Values need not to be repeated at Room Temperature Electrical Measurements.
5. Check for lot failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Para 8.9.1, 8.9.2, 8.9.3 subsequent to HTRB Burn-In.
6. Performed on sample basis.
12.4 CHART F4: CAPABILITY APPROVAL, CAPABILITY APPROVAL MAINTENANCE AND LOT VALIDATION TESTS

50 (1) Test Structures or Components (2)

Subgroup 1
Environmental/Mechanical
24 Months Period

15 (1) Test Structures or Components

Mechanical Shock
Para. 8.11

Vibration
Para. 8.12

Constant Acceleration
Para. 8.13

Seal
Para. 8.8.1 and Para. 8.8.2

Intermediate and End Point Electrical Measurements
Para. 8.9.4

External Visual Inspection
Para. 8.10

Subgroup 2
Endurance
12 Months Period

15 (1) Test Structures or Components

Thermal Shock
Para. 8.14

Moisture Resistance
Para. 8.15

Seal
Para. 8.8.1 and Para. 8.8.2

Intermediate and End Point Electrical Measurements
Para. 8.9.4

External Visual Inspection
Para. 8.10

Subgroup 3
Assembly/Capability
24 Months Period

15 (1) Test Structures or Components

Operating Life
2000 Hours
Para. 8.19

Intermediate and End Point Electrical Measurements
Para. 8.9.4

Seal
Para. 8.8.1 and Para. 8.8.2

External Visual Inspection
Para. 8.10

5 (1) Test Structures or Components

Terminal (3) Strength
Para. 8.18

Internal Visual Inspection
Para. 8.1

Bond Strength
Para. 8.2.1

Die Shear
Para. 8.2.2

Notes to Chart F4:
1. For distribution within the subgroups see Para. 7.1.2 or Para. 7.4.2 (as applicable).
2. No failures are permitted.
3. May be done at the beginning or the end of the subgroup, depending on package configuration.