N-CHANNEL POWER MOSFET

BASED ON TYPE L4002

DLR Detail Specification No DLR-RF-PS-STD-013

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DOCUMENTATION CHANGE NOTE

Rev. Letter	Rev. Date	CHANGE Reference Item	Approved DCR No.
2	March 2014	- Paragraph 3: Abbreviation and term of “PID” added. - Paragraph 4.2.1: Deviation in production control Chart F2 of DLR-RF-PS-STD-006: Additional components without coating shall be produced to enable Bond- Strength test in Subgroup 3. - Paragraph 4.2.2: An initial electrical measurement according table 2a and 2b was implemented with start of the screening. - Paragraph 4.2.2: In case that the radiographic inspection occurs after the electrical measurement (paragraph 8.9.3 of Generic Specification) an additional electrical measurement to confirm ESD protected handling has to be performed. - Paragraph 4.2.3: Subgroup 2(A) consists of 10 samples for Operating Life Test. Subgroup 2(B) has to be charged with 5 coated and 5 not-coated samples for Intermitted Power Cycles Test. Electrical measurements are performed at start, also after 2000 and 6000 cycles. Conditions as specified in table 5(c) and 5(d). - Paragraph 4.2.3: If subgroup 2(B) has been finished, subgroup 3 is charged by 5 not coated samples of subgroup 2(B) - Paragraph 4.2.4: Definition of Bond Strength Test moved from paragraph 4.2.3 to paragraph 4.2.4. - Paragraph 4.2.4: Deviation to paragraph 8.6 of Generic Specification revised: Conditions for the Thermal Cycling test as specified in table 1b maximum ratings. - Paragraph 4.2.4: Failure criteria after moisture resistance test (DLR-RF-PS-STD-006, paragraph 8.15) allowed as specified in MIL-STD-750, TM 1021. - Paragraph 4.2.4: Definition of duration while HTRB test (DLR-RF-PS-STD-006, paragraph 8.20) shifted from paragraph 4.2.2 to paragraph 4.2.4. - Paragraph 4.3.4: Internal cavity coating process described more detailed to chronology and in accordance to manufacturer’s PID. - Table 5(d) Conditions for Intermittent Power Cycles: Parameter 5: Initial “Drain current” reduced from 0,15A to 0,14A. Prefix of default drain current changed from minimum (min) to typically (typ.). The final current results by adjustment of the specified junction temperature Tj. (Estimated/calculated values range Id ~ 0.145 A – 0,15A).	
		Remarks:	

TABLE OF CONTENTS

1 General 4
1.1 Scope 4
1.2 Component Type Variants 4
1.3 Maximum Ratings 4
1.4 Parameter Derating Information 4
1.5 Physical Dimensions 4
1.6 Functional Diagram 4
1.7 Handling Precautions 4
1.7.1 ESD Precaution 4
1.7.2 Electrical Precaution 4
2 Applicable Documents 10
3 Terms, Definitions, Abbreviations, Symbols and Units 10
4 Requirements 11
4.1 General 11
4.2 Deviations / Amendments from Generic Specification DLR-RF-PS-STD-006 11
4.2.1 Deviations from Production Controls (Chart F2) 11
4.2.2 Deviations from Screening Tests (Chart F3) 11
4.2.3 Deviations from Capability Approval, Capability Approval Maintenance and Lot Validation test (Chart F4) 11
4.2.4 Deviations from Test Methods and Procedures (paragraph 8) 11
4.3 Mechanical Requirements 12
4.3.1 Dimension Check 12
4.3.2 Weight 12
4.3.3 Terminal Strength Test 12
4.3.4 Coating of internal cavity 12
4.4 Materials and Finishes 12
4.4.1 Case 12
4.4.2 Terminal Material and Finishes 13
4.5 Marking 13
4.5.1 General 13
4.5.2 Lead Identification 13
4.5.3 DLR Component Number 13
4.6 Electrical Measurements 13
4.6.1 Electrical Measurements at Room Temperature 13
4.6.2 Electrical Measurements at High and Low Temperatures 13
4.6.3 Circuits for Electrical Measurements 13
4.7 Screening Tests 13
4.7.1 Parameter Drift Values 13
4.7.2 Conditions for High Temperature Reverse Bias Burn-In (HTRB) 13
4.7.3 Conditions for High Temperature Gate Bias Burn-In (HTGB) 13
4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-In (HTRB) 14
4.7.5 Electrical Circuit for High Temperature Gate Bias Burn-In (HTGB) 14
4.7.6 Verification of Safe Operating Area 14
4.8 Environmental / Mechanical, Endurance Tests and Assembly and Capability Test (Chart F4 of DLR-RF-PS-STD-006) 20
4.8.1 Electrical Measurements on Completion of Environmental Tests 20
4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests 20
4.8.3 Electrical Circuit for Operating Life Tests 20
4.8.4 Electrical Circuit for Intermittent Power Cycles Measurements 20
4.8.5 Conditions for Operating Life Tests 20
4.8.6 Conditions for Intermittent Power Cycles 20
4.9 Total Dose Irradiation Testing 20

1 General

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data for N-Channel Power MOSFET, based on LEWICKI Type L4002 (based on IRFC310).
It shall be read in conjunction with DLR Generic Specification DLR-RF-PS-STD-006, the requirements of which are supplemented herein.

1.2 Component Type Variants

Variants of the basic type transistors specified herein, which are also covered by this specification, are listed in table 1(a).

1.3 Maximum Ratings

The maximum ratings for the Power MOSFET specified herein, which shall not be exceeded at any time during use or storage, are as scheduled in table 1(b).

1.4 Parameter Derating Information

The parameter derating information for the Power MOSFET specified herein is shown in figure 1(a). The Safe Operating Area information is shown in figure 1(b).

1.5 Physical Dimensions

The physical dimensions for the Power MOSFET specified herein are shown in figure 2.

1.6 Functional Diagram

The functional diagram for the Power MOSFET specified herein, including lead identification, is shown in figure 3.

1.7 Handling Precautions

1.7.1 ESD Precaution

The Power MOSFET specified herein is susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling. Power MOSFET is categorized in class 1, with a minimum critical path failure voltage of 250V.

1.7.2 Electrical Precaution

Never insert the MOSFET into the circuit when voltage is applied. When applying bias to the MOSFET first apply gate voltage then drain voltage. Avoid turning the instrument power on and off or switching between instrument ranges when bias is applied to the MOSFET. Transient generated in the vicinity must be eliminated.

Table 1(a) – Type Variants

	(01)	(02)	(03)	(04)	(05)	(06)	(07)	(08)	(09)	(10)
Variant / Type Note 1	Package Type	Based on Type	ID (MAX.) [A] Note 2	ID (MAX.) [A] Note 3	IS [A] Note 2	VDS [V]	IDM(MAX) [Apk] Note 4	VDG [V]	Ptot [W] Note 2	RTH (J-C) [K/W]
01	Intentional left blank									
02	SMD05	IRFC310	1.7	1.1	1.7	400	6	400	50	2,5

NOTES:

1. Variant 02 = L4002-005
2. Tcase = 25 ℃ (thermally conductive mounted to a liquid cooled copper heat sink)
3. Tcase = 100 ℃ (thermally conductive mounted to a liquid cooled copper heat sink)
4. Repetitive rating; pulse width limited by maximum junction temperature

Table 1(b) – Maximum Ratings

No.	Characteristics	Symbol	Maximum Ratings	Unit	Remarks
1	Drain Source Voltage	VDS	400	V	
2	Gate Source Voltage	VGS	+/- 20	V	
3	Drain Gate Voltage	VDG	Table 1(a) Column (08)	V	
4	Drain Current (Continuous)	ID	Table 1(a) Column (03)	A	at Tcase=+25 ℃
5	Drain Current (Continuous)	ID	Table 1(a) Column (04)	A	at Tcase=+100 ℃
6	Source Current (Continuous)	IS	Table 1(a) Column (05)	A	at Tcase =+25 ℃
7	Drain Current Pulsed (Peak)	IDM	Table 1(a) Column (07)	Apk	
8	Total Power Dissipation	Ptot	Table 1(a) Column (9)	W	Note 1
9	Operating Temperature Range	Top	-55 to +150	℃	Ta mb
10	Storage Temperature Range	Tsto	-55 to +150	℃	
11	Soldering Temperature	Tsol	+260	℃	Note 2
12	Thermal Resistance (Junction to Case)	Rth(J-C)	Table 1(a) Column (10)	K/W	

NOTES:

1. For derating, see figure 1(a)
2. Duration 10 seconds maximum. The same termination shall not be resoldered until 3 minutes have elapsed

Figure 1(a) – Parameter Derating Information
Variant 02

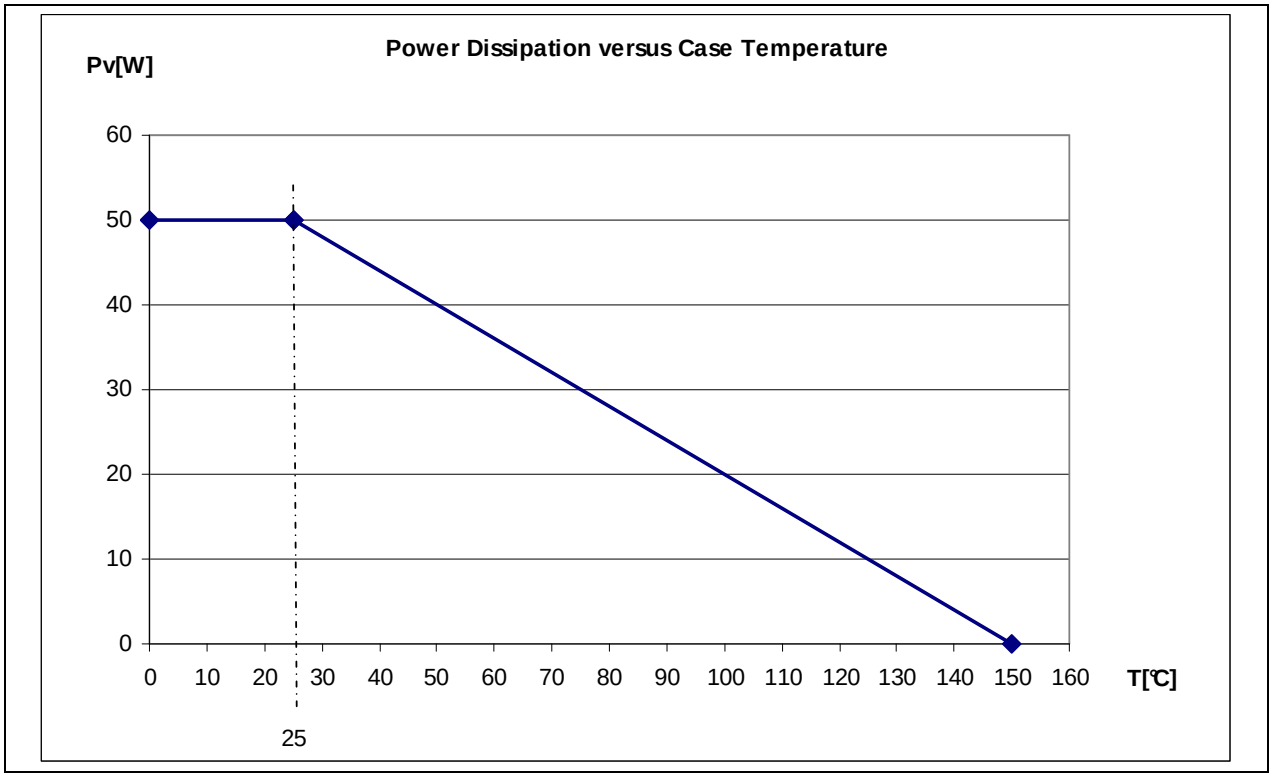


Figure 1(b) – Maximum Safe Operating Area (Devices mounted without heat sink)
Variant 02

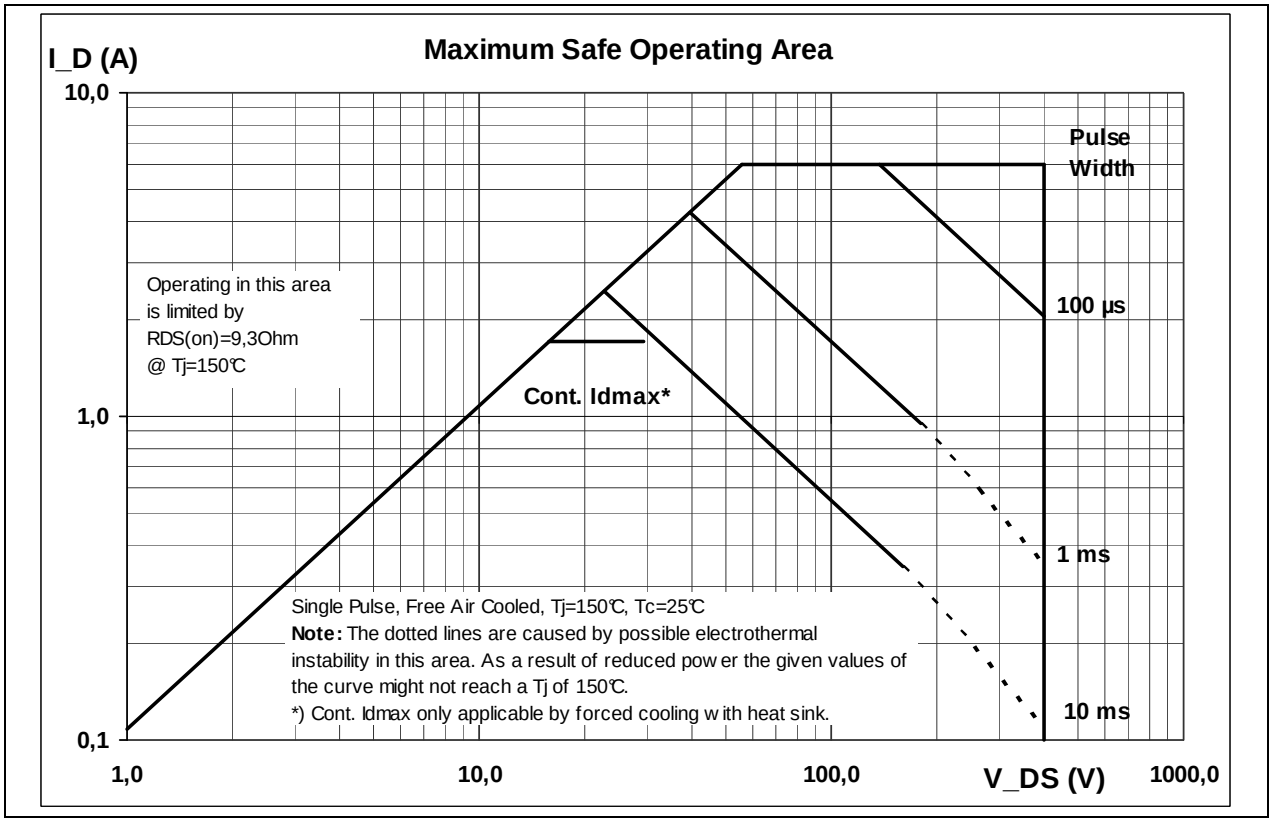
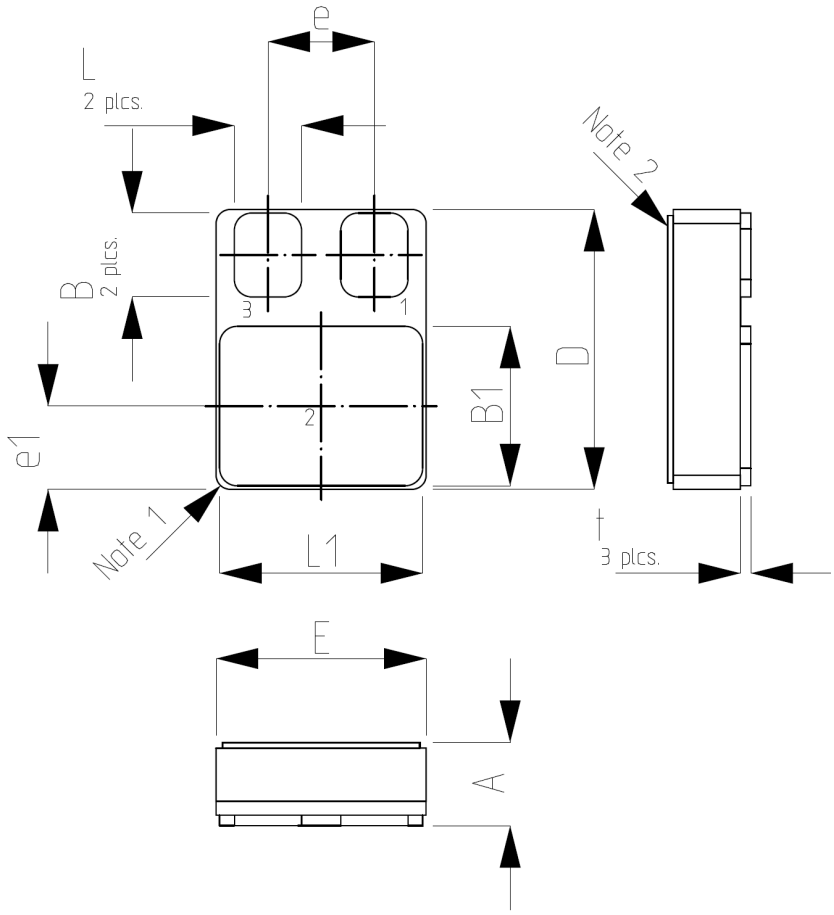


Figure 2 – Physical Dimensions
Variant 02

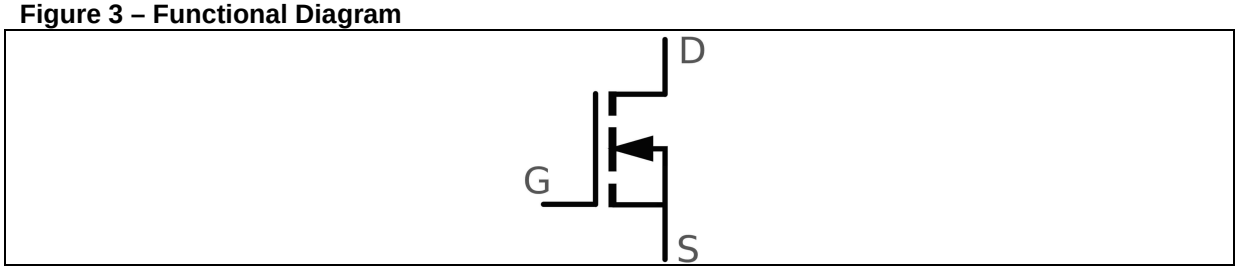


Pos.	Symbol	Dimensions [mm]	
		Min.	Max.
1	A	2.71	3,15
2	B	2.92	3.18
3	B1	5.59	5.85
4	D	10.03	10.29
5	E	7.41	7.67
6	e	3.68	3.94
7	e1	2.86	3.12
8	L	2.29	2.54
9	L1	7.13	7.39
10	t	0.25	0.50

NOTES:

1. Corner radii from R0.3 to R0.7
2. Marking according to paragraph 4.5

Figure 3 – Functional Diagram



Terminal	**Variant 02** L4002-005
1	Gate
2	Drain
3	Source

NOTES:

1. Variant 02 (L4002-005): Due to the insert Al2O3 packages the drain is electrically isolated from the case.

2 Applicable Documents

The following specifications and standards form a part of this specification to the extend specified herein.

1	DLR-RF-PS-STD-006	Discrete Semiconductor Components
2	ESCC 20900	Radiographic Inspection of Electronic Components
3	ESCC 2095000	Radiographic Inspection of discrete Semiconductors
4	ESCC 21300	Terms, Definition, Abbreviations Symbols and Units
5	ESCC 21700	General Requirements for the Marking of ESCC Components
6	ESCC 23500	Requirements for Lead Materials and Finishes for Components for Space Application
7	MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
8	MIL-STD-750	Test Methods and Procedures for Semiconductor Devices
9	MIL-STD-883	Test Methods Standards, Microcircuits

3 Terms, Definitions, Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definition, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

BVGSS	Gate to Source Breakdown Voltage
BVDSS	Drain to Source Breakdown Voltage
CISS	Common Source Input Capacitance
COSS	Common Source Output Capacitance
CrSS	Common Source Output Transfer Capacitance
DUT	Device under test
ESCC	European Space Components Coordination
gfs	Forward Transfer Conductance
HTGB	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
ID	Drain Current
IGSS	Gate to Source Leakage Current
IS	Source Current
MIL – STD, TM	Military Standard, Test Method
PID	Process Identification Document
Ri	Insulated Resistance, Terminals to case
SMD	Surface Mounted Device
SOA	Safe Operating Area
VDG	Drain to Gate Voltage
VDS	Drain to Source Voltage
VGS	Gate to Source Voltage
VGS(th)	Gate Threshold Voltage
VSD	Source to Drain Diode Forward Voltage

4 Requirements

4.1 General

The complete requirements for procurement of the Power MOSFET specified herein are stated in this specification and Generic Specification DLR-RF-PS-STD-006 for discrete semiconductor components. Deviations from the Generic Specification DLR-RF-PS-STD-006 applicable to this specification are listed in the following paragraph 4.2.

4.2 Deviations / Amendments from Generic Specification DLR-RF-PS-STD-006

4.2.1 Deviations from Production Controls (Chart F2)

- Wafer Lot Acceptance Test is replaced by an Incoming Inspection at the Assembly & Testhouse. Incoming Inspection shall be in accordance with DLR-RF-PS-STD-006 paragraph 4.7.9. Hereby the visual inspection is performed on all samples (100 % inspection) and the die attach and bondability is tested on 3 samples. The Bond Strength Test of paragraph 8.2.1 is performed in accordance to referenced MIL-STD-750, TM 2037 Condition D instead of condition A or B.
- After completion of pre-encapsulation inspection, DLR-RF-PS-STD-006, paragraph 5.3.2 a coating as specified in paragraph 4.3.4 of this specification shall be applied.
- For further Bond Strength Tests of subgroup 3, Chart F4 an adequate number of samples shall be produced without coating (this deviation relates also to paragraph 4.7.6 of DLR-RF-PS-STD-006 including different lot identifiers for coated and uncoated parts).

4.2.2 Deviations from Screening Tests (Chart F3)

- With start of the screening an additional initial electrical measurement according to table 2a and 2b of the Detail Specification has to be performed as notified with paragraph 8.9.3. of Generic Specification DLR-RF-PS-STD-006.
- In case that the radiographic inspection of paragraph 8.23 of Generic Specification DLR-RF-PS-STD-006 occurs after step Electrical Measurements (paragraph 8.9.3 of Generic Specification), an electrical measurement after the radiographic inspection according to table 2a of the Detail Specification has to be performed.
- The Power Burn-In of paragraph 8.21 of Generic Specification is replaced by HTGB as specified in table 5(b) herein.
- The PIND test as described in paragraph 8.7 of the Generic Specification is not applicable since the type is internally coated (see paragraph 4.3.4 herein).
- The Radiographic Inspection of paragraph 8.23, DLR-RF-PS-STD-006, focuses only on the die attach area with respect to excess of contact area voids. Other named failure criteria in paragraph 4.3 of ESCC No. 2095000 are inspected with Pre-encapsulation Inspection of paragraph 5.3.2 of DLR-RF-PS-STD-006.

4.2.3 Deviations from Capability Approval, Capability Approval Maintenance and Lot Validation test (Chart F4)

- The sample size from subgroup 2 will be increased from 15 to 20 samples.
- Subgroup 2 is divided into subgroup 2(A) Operation Life with 10 samples and subgroup 2(B) Intermittent Life with 10 samples. Subgroup 2(B) consists of 5 coated and 5 not-coated samples (see paragraph 4.2.1 above). In Subgroup 2(B) measurements are performed after 0, 2000 and 6000 cycles. Conditions see table 5(c) and table 5(d).
- After completion of subgroup 2, 5 not-coated test samples from subgroup 2(B) are used for subgroup 3.
- Permanence of marking of paragraph 8.17 of Generic Specification is not applicable.

4.2.4 Deviations from Test Methods and Procedures (paragraph 8 of Generic Specification)

- The Bond Strength Test of paragraph 8.2.1 of DLR-RF-PS-STD-006 is performed in accordance to referenced MIL-STD-750, TM 2037 Condition D instead of condition A or B.

- For the Thermal Cycling test of paragraph 8.6 of Generic Specification the maximum storage temperature range as specified in table 1b of this document has to be applied.
- For the final External Visual Inspection paragraph .8.10. in subgroup 1 with the moisture resistance test paragraph 8.15 of the Generic Specification DLR-RF-PS-STD-006 failure criteria as specified in MIL-STD-750 Method 1021 are allowed.
- The Vibration Test of paragraph 8.12 of DLR-RF-PS-STD-006 is performed in the frequency range 100Hz-2000Hz-100Hz in accordance to the referenced MIL-STD-750, TM2056.
- The Constant Acceleration stress level test as described in paragraph 8.13 of the Generic Specification is not applicable since the type is internally coated.
- The HTRB of paragraph 8.20 of Generic Specification is performed for 168 h instead of 48 h

4.3 Mechanical Requirements

4.3.1 Dimension Check

The dimensions of the Power MOSFET specified herein shall be checked on sample base. They shall conform to those shown in figure 2.

4.3.2 Weight

The maximum weight of the Power MOSFET specified herein is:

Type	Package	Weight [g]
L4002-005	SMD05	1.1

4.3.3 Terminal Strength Test

For Terminal Strength Test a solid copper wire is soldered to the pad respectively the specified weight shall be applied to each lead. The requirements are specified in MIL-STD-883 TM 2004, test condition D (solder pad adhesion for leadless chip carrier and similar devices) and is applicable. The applied force and duration are as follows:
Variant 02: Applied force 10 N, duration 30 s

4.3.4 Coating of internal cavity

Internal cavity coating is applied on all electric conductive surfaces inside the package after customer pre-encapsulation inspection and prior to encapsulation as specified in the manufacturer's PID. The coating has to be applied in such a way that in the critical pressure range (10 torr – 10xE-2 torr) inside the cavity at the specified rated voltage no discharge will occur.

4.4 Materials and Finishes

The material and finish shall be as specified herein. Where a definite material is not specified, a material which will enable the MOSFET specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

Package	Type	Materials and finishes
SMD05	L4002-005	Body: ceramic Al2O3 Frame: Kovar Au plate 1.27 µm min over 2.54 µm Ni
		Lid: Kovar Au plate 1µm max over min 3.8 µm Ni

The package is hermetically sealed: 1E-08 atm cc / s

4.4.2 Terminal Material and Finishes

The terminal material is CuW and in accordance with the requirements of ESCC Basic Specification No. 23500 type 'Q' and type '14' finish. Terminals are plated with min 1.27µm Au over min 2.54µm Ni.

4.5 Marking

4.5.1 General

The component specified herein is marked in accordance with the requirements of ESCC Basic Specification No. 21700. The information to be marked and the order of precedence are as follows:

- DLR Component Number
- DLR Logo (in case the part is covered by the capability approval)
- Traceability Information

4.5.2 Lead Identification

Lead Identification shall be as in figure 2 and figure 3.

4.5.3 DLR Component Number

Each component shall bear the DLR component number which shall be constituted and marked as follows:

DLR-RF-PS-STD-013	-	0X
DLR component number		Variant Identification 02 = L4002-005

4.6 Electrical Measurements

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in table 2 and table 6. Unless otherwise specified, the measurements have been performed at Tamb = 25℃ +/- 5℃.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured in respect of electrical characteristics are scheduled in table 3. The measurements have been performed at Tamb = 125 ℃ + 0 ℃/-5 ℃ and Tamb = -55 ℃ +5 ℃/-0 ℃ respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements are listed in figure 4 of this specification.

4.7 Screening Tests

4.7.1 Parameter Drift Values

The parameter drift values applicable to Burn-In are specified in table 4 of this specification. Unless otherwise stated, measurements shall be performed at Tamb = 25 ℃ +/- 5 ℃. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift values requirements, the appropriate limit value specified for a given parameter in table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-In (HTRB)

The requirements for the HTRB Burn-In are specified in MIL-STD-750 TM 1042 test condition A (steady – state gate bias) and as specified in table 5(a) of this specification.

4.7.3 Conditions for High Temperature Gate Bias Burn-In (HTGB)

The requirements of the HTGB Burn-In are specified in MIL-STD-750 TM 1042 test condition B (steady – state gate bias) and as specified in table 5(b) of this specification.

4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-In (HTRB)

The electrical circuit for HTRB is shown in figure 5(a) of this specification.

4.7.5 Electrical Circuit for High Temperature Gate Bias Burn-In (HTGB)

The electrical circuit for HTGB is shown in figure 5(b) of this specification.

4.7.6 Verification of Safe Operating Area

As specified in paragraph 8.22 of Generic Specification the test is performed in accordance with MIL-STD-750 TM 3474 and as specified below. Figure 4(a) shows the electrical circuit for verification of SOA. At the case temperature Tc = 25 ℃ ten pulses for the maximum allowed current at VDS = 80% of the maximum rated VDS and at 10ms as given in figure 1(b) has to be applied. The device has no contact to an additional heat sink, but has to be cooled by free-air only. The time between each pulse shall such that the part can cool down at room temperature. After 10 pulses are applied table 2(a) except no. 9 shall be measured. All failed parts shall be removed from the lot.

Table 2(a) – Electrical Measurements at Room Temperature / DC Parameters

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
1	Breakdown Voltage Drain Source	BVDSS	3407 Bias Condition ‘C’	ID=250 µA VGS=0 V	400	-	V
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS	2	4	V
3	Forward Gate to Source Leakage Current	IGSSF	3411	VGS=20 V	-	100	nA
4	Reverse Gate to Source Leakage Current	IGSSR	3411	VGS=-20 V	-100	-	nA
5	Drain Current	IDSS	3413 Bias Condition ‘C’	VGS=0 V VDS=Note 2	-	25	µA
6	Drain Source On Resistance	RDS(ON)	3421	ID=1 A VGS=10 V Note 1	-	3.6	Ω
7	Drain Source On Voltage	VDS(ON)	3405	ID=1 A VGS=10 V Note 1	-	3.6	V
8	Source to Drain Diode Forward Voltage	VSD	4011	IS= 1.7 A VGS=0 V Note 1	-	1.6	V
9	Insulation Resistance	Ri	MIL-STD-202 TM302 Condition ‘C’	Note 3	100	-	MΩ

NOTES:

1. Pulsed measurement: pulse width ≤ 100 µs, duty cycle ≤ 1 %
2. VDS (80 %) = 320 V
3. Between linked terminals and case
4. Table 2(b):Thermal Impedance has to measured only one time device mounted in plug base, without forced cooling

Table 2(b) – Electrical Measurements at Room Temperature / AC Parameters

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
10	Forward Transconductance	gfs	3475	ID=1 A VDS=50 V Note 1	0.5	-	S
11	Turn-on Delay Time	td(ON)	3472 and figure 4(b) below	RD=100 Ω ID=2A VGS=0 V / 10 V VDD=200 V	-	16	ns
12	Rise Time	tr	3472 and figure 4(b) below	RD=100 Ω ID=2A VGS=0 V / 10 V VDD=200 V	-	20	ns
13	Turn-off Delay Time	td(OFF)	3472 and figure 4(b) below	RD=100 Ω ID=2A VGS=0 V / 10 V VDD=200 V	-	42	ns
14	Fall Time	tf	3472 and figure 4(b) below	RD=100 Ω ID=2A VGS=0 V / 10 V VDD=200 V	-	25	ns
15	Common Source Input Capacitance	Ciss	3431	VDS=25 V VGS=0 V f=1 MHz	-	250	pF
16	Common Source Output Capacitance	Coss	3453	VDS=25 V VGS=0 V f=1 MHz	-	70	pF
17	Common Source Reverse Transfer Capacitance	Crss	3433	VDS=25 V VGS=0 V f=1 MHz	-	25	pF
18	Thermal Impedance	Zth	3161	tH=10 ms tMD=30 µs tSW=10 µs IH=1 A VH=30 V Note 4 Variant 02	-	2	K/W
19	Thermal Impedance	Zth	3161	tH=30 ms tMD=30 µs tSW=10 µs IH=1 A VH=30 V Note 4 Variant 02	-	3,3	K/W

Table 3(a) – Electrical Measurements at High Temperature (Ta = 125 ℃ +0 ℃/-5 ℃)

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS	2	4	V
3	Forward Gate to Source Leakage Current	IGSSF	3411	VGS=20 V	-	250	nA
4	Reverse Gate to Source Leakage Current	IGSSR	3411	VGS=-20 V	- 250	-	nA
5	Drain Current	IDSS	3413 Bias Condition 'C'	VGS=0 V VDS=Note 2	-	250	µA
6	Drain Source On Resistance	RDS(ON)	3421	ID=1 A VGS=10 V Note 1	-	7.8	Ω

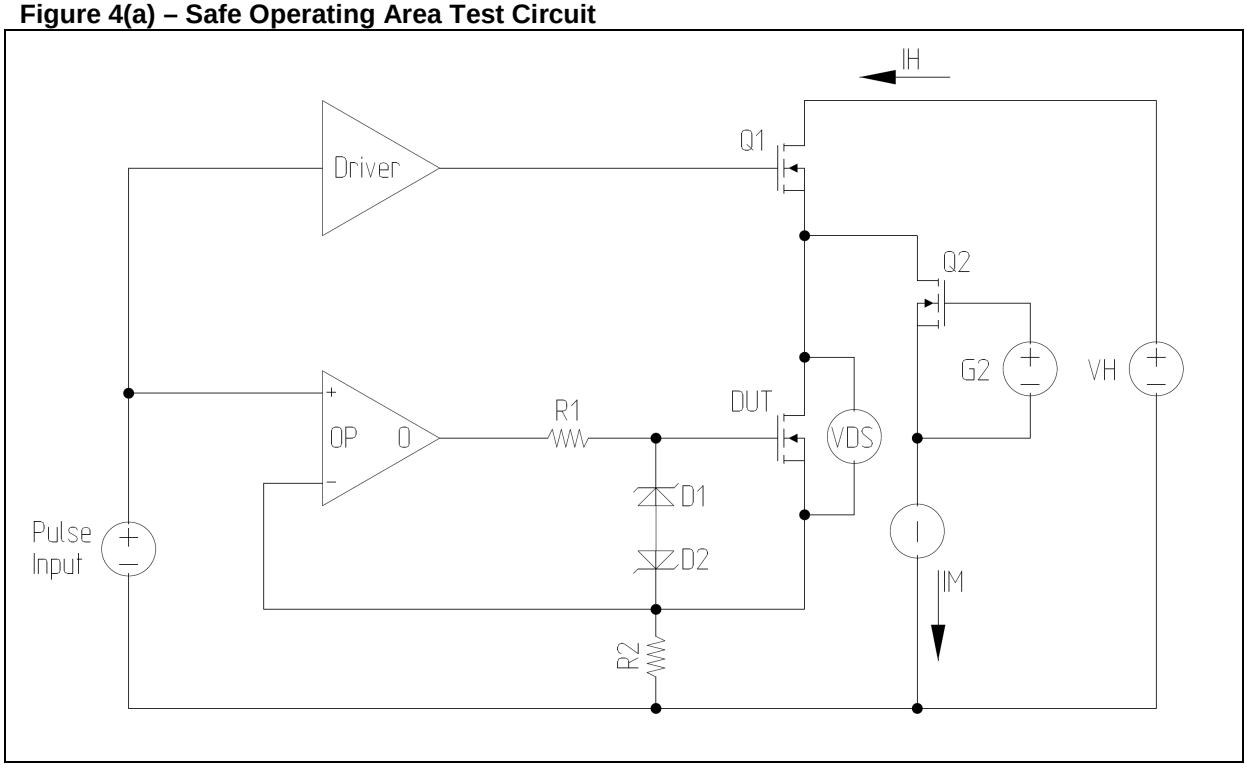
NOTES: see Notes of table 2(a)

Table 3(b) – Electrical Measurements at Low Temperature (Ta = -55 ℃ -0 ℃/+5 ℃)

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
2	Gate Threshold Voltage	VGS(th)	3403	ID=250 µA VDS=VGS	2	5	V

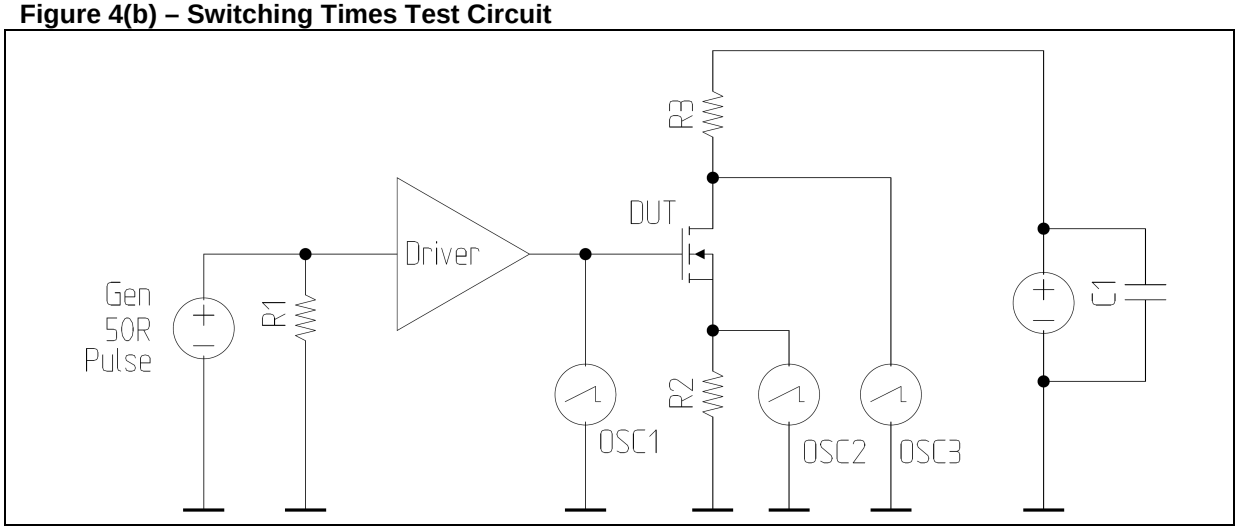
NOTES: see Notes of table 2(a)

Figure 4 – Circuits for Electrical Measurements
Figure 4(a) – Safe Operating Area Test Circuit



IH = Heat Current; VH = Heat Voltage
Pulse Input: as specified in Paragraph 4.7.6

Figure 4(b) – Switching Times Test Circuit



C1: Voltage Source buffer
OSC1 – OSC3: Oscilloscope 1 – 3
OSC1: VGS(ON) and VGS(OFF), OSC3: VDS(ON) and VDS(OFF)
Pulse Input: < 100 µs

Switching Time Test Signals

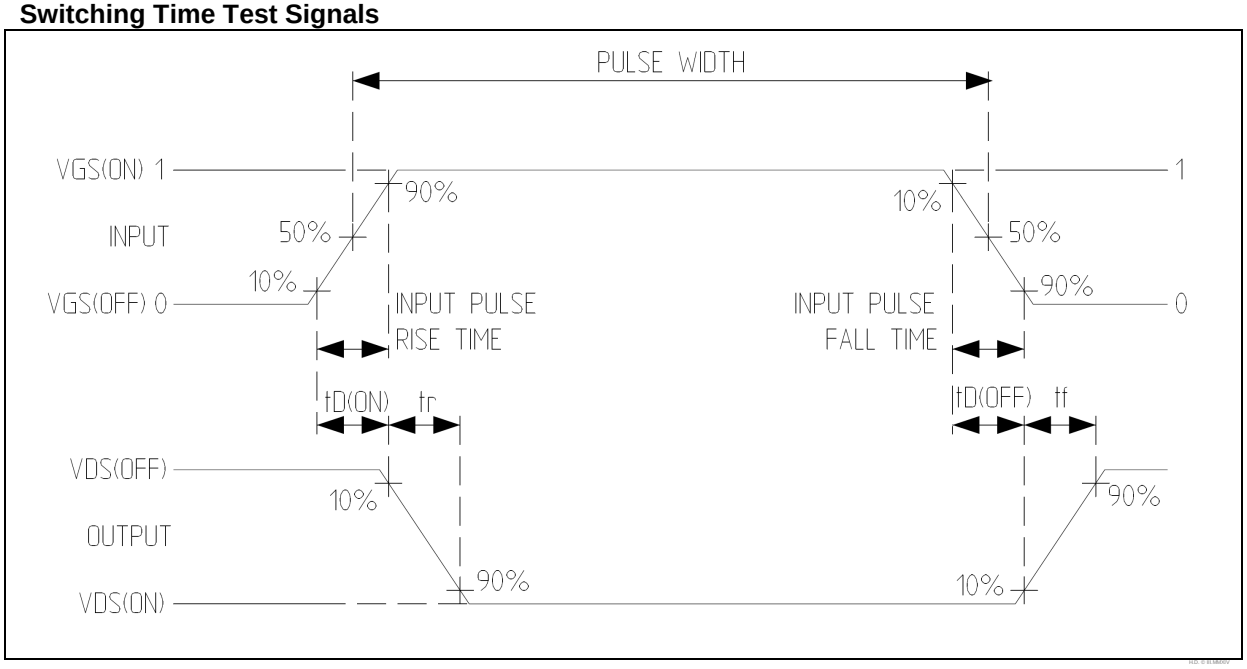


Table 4 – Parameter Drift Values

No.	Characteristics	Symbol	Spec. and/or Test Method	Test Conditions	Change Limits (Δ)	Unit
2	Gate Threshold Voltage	VGS(th)	As per table 2	As per table 2	-20 / 20	%
3	Forward Gate to Source Leakage Current	IGSSF	As per table 2	As per table 2	-20 / 20	nA
4	Reverse Gate to Source Leakage Current	IGSSR	As per table 2	As per table 2	-20 / 20	nA
5	Drain Current	IDSS	As per table 2	As per table 2	-10 / 10	µA
6	Drain Source On Resistance	RDS(ON)	As per table 2	As per table 2	-20 / 20	%

Table 5(a) – Conditions for High Temperature Reverse Bias (HTRB)

No.	Characteristics	Symbol	Conditions	Unit
1	Ambient Temperature	Tamb	+150 (+0 / -10)	℃
2	Drain Source Voltage	VDS	320	V
3	Gate Source Voltage	VGS	0	V
4	Duration	t	168	h

Table 5(b) – Conditions for High Temperature Gate Bias (HTGB)

No.	Characteristics	Symbol	Conditions	Unit
1	Ambient Temperature	Tamb	+150 (+0 / -10)	℃
2	Drain Source Voltage	VDS	0	V
3	Gate Source Voltage	VGS	16	V
4	Duration	t	48	h

Table 5(c) – Conditions for Operating Life Test (Note 1)

No.	Characteristics	Symbol	Conditions	Unit
1	Junction Temperature	TJ	+140 – +150	℃
2	Power Dissipation	PD	Variant 02: Min. 36 (Note 2)	W
3	Duration	t	2000	h

Table 5(d) – Conditions for Intermittent Power Cycles

No.	Characteristics	Symbol	Conditions	Unit
1	Junction Temperature	TJ	+125 (+15 / -10)	℃
2	Heating time	t(ON)	10	s
3	Cycles		6000	
4	Drain Source Voltage	VDS	24-28	V
5	Drain Current	ID	Variant 02: typ. 0.14 (Note 3)	A

NOTES:

1. Using the circuit in figure 5(c), power shall be applied to the device.
   Parts shall be thermally conductive mounted to a liquid cooled heat sink so that the specified junction temperature (TJ) will be reached.
   The junction temperature (TJ) should be determined by measurement of the reverse diode.
2. Minimum power dissipation to be adjusted to get the specified junction temperature (TJ). The power dissipation shall not be below the minimum value.
3. Initial value of drain current adjusted to the specified junction temperature (TJ). The junction temperature (TJ) should be determined by measurement of the reverse diode.

Figure 5(a) – Electrical Circuit for High Temperature Reverse Bias (HTRB) Burn In

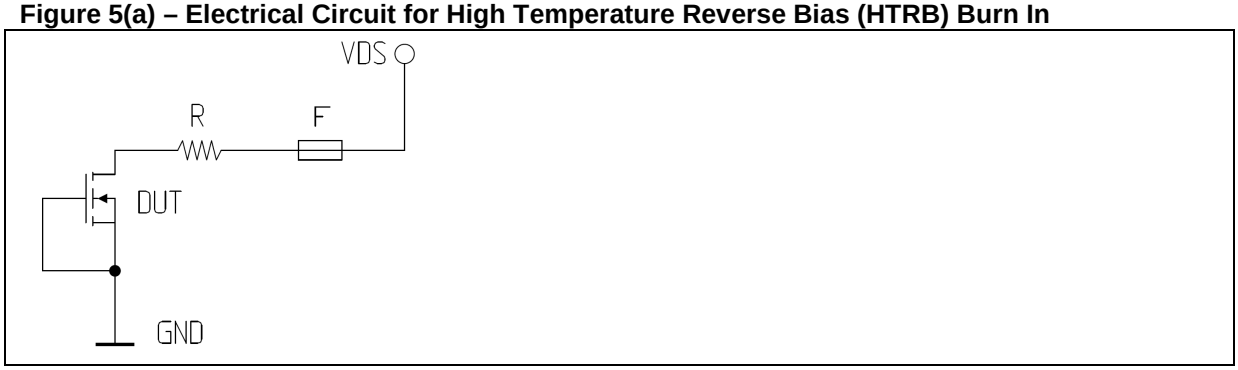


Figure 5(b) – Electrical Circuit for High Temperature Gate (HTGB) Burn In

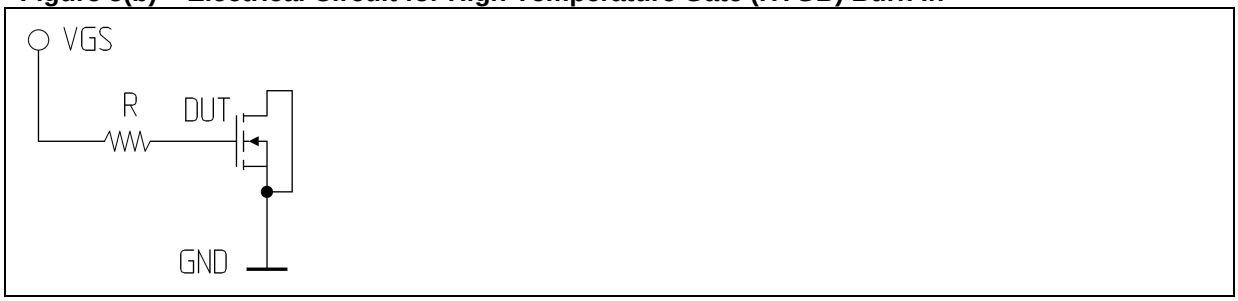


Figure 5(c) – Electrical Circuit for Operating Life Test

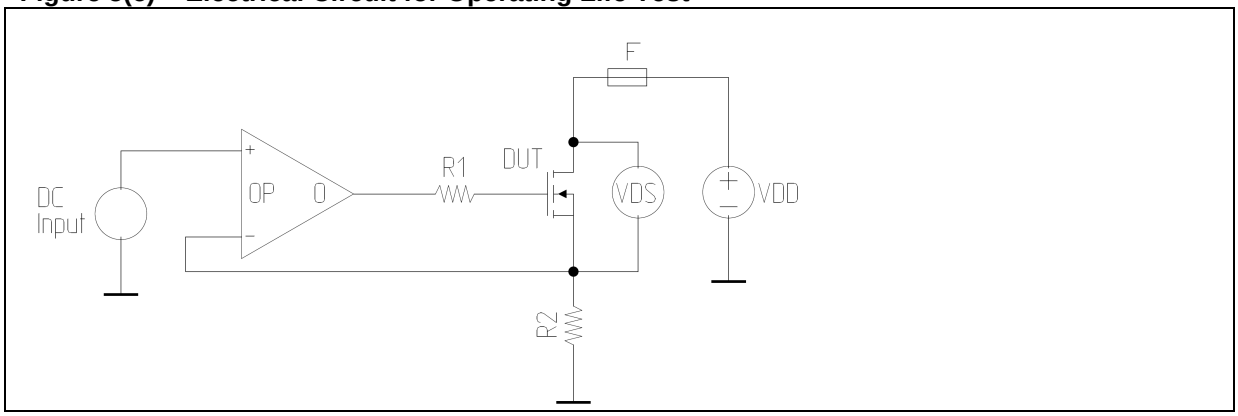
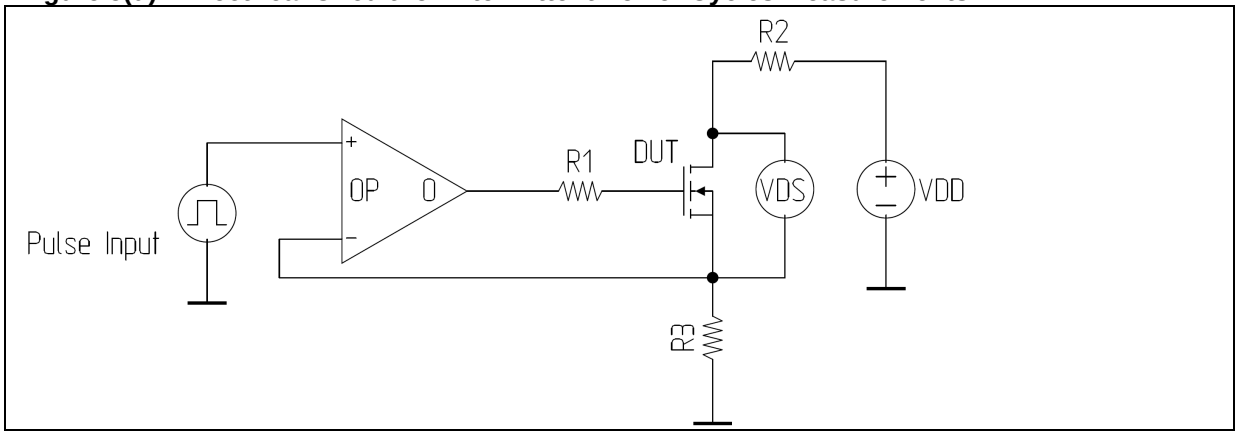


Figure 5(d) – Electrical Circuit for Intermittent Power Cycles Measurements



IH = Heat Current, VH = Heat Voltage

4.8 Environmental / Mechanical, Endurance Tests and Assembly and Capability Test (Chart F4 of DLR-RF-PS-STD-006)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are schedule in table 2 of this specification. Unless otherwise stated, the measurements shall be performed at Tamb = 25℃ +/- 5℃.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in table 6 of this specification. Unless otherwise stated, the measurements shall be performed at Tamb = 25 ℃ +/- 5 ℃.

4.8.3 Electrical Circuit for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in figure 5(c) of this specification.

4.8.4 Electrical Circuit for Intermittent Power Cycles Measurements

The circuit to be used for performing the intermittent measurements shall be the same as shown in figure 5(d) of this specification.

4.8.5 Conditions for Operating Life Tests

The requirements of operating life testing are specified in paragraph 8.19 of DLR Generic Specification no. DLR-RF-PS-STD-006 and amended of paragraph 4.2.3. The conditions for operating life testing shall be the same as specified in table 5(c) of this specification.

4.8.6 Conditions for Intermittent Power Cycles

The requirements for intermittent power cycles are specified in MIL-STD-750 TM 1042, test condition ‘D’ and amended of paragraph 4.2.3. The conditions shall be the same as specified in table 5(d) of this specification.

Table 6 – Electrical Measurements of Intermediate Points and on Completion of Endurance Testing

No.	Characteristics	Symbol	MIL-STD-750 Test Method	Test Conditions	Limits		Unit
					Min.	Max.	
1	Gate Threshold Voltage	VGS(th)	As per table 2	As per table 2	2	4	V
2	Forward Gate to Source Leakage Current	IGSSF	As per table 2	As per table 2	-	100	nA
3	Reverse Gate to Source Leakage Current	IGSSR	As per table 2	As per table 2	-100	-	nA
4	Drain Current	IDSS	As per table 2	As per table 2	-	25	µA

4.9 Total Dose Irradiation Testing

Not applicable